MOTOROLA

MCM14537

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input (WE), one strobe input (ST), two chip enable inputs (CE_n), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The CE and ST inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When CE2 is high the chip is fully disabled. When CE1 is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the CE1 input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the CE and ST lines.

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

- Quiescent Current = 0.5 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

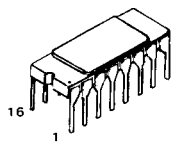
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY

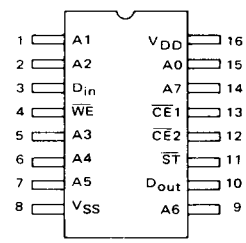


CERAMIC PACKAGE
CASE 690

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
(V_{out} = 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} = 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} = 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
(V_{out} = 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} = 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} = 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±1.0		±0.00001	±1.0	–	±14	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–		5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0		100		0.5	100	–	1800	µAdc
		10		200		1.0	200	–	3600	
		15		400		1.5	400	–	7200	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	µAdc
		10	–	200	–	1.0	200	–	3600	
		15	–	400	–	1.5	400	–	7200	
Total Supply Current** † (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.91 µA/kHz) f + I_{DD}							
		15	I_T = (4.37 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15		±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15		±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

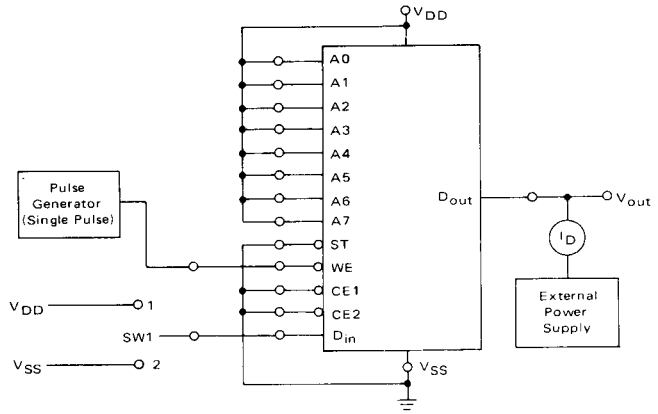
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	3	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	3	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Access Time from $\overline{ST}$ or $\overline{CE}2$	4, 5	$t_{acc(R)}$					ns
t_{acc} = (1.4 ns/pF) C_L + 2480 ns			5.0	400	2500	6000	
t_{acc} = (0.7 ns/pF) C_L + 690 ns			10	150	700	2000	
t_{acc} = (0.5 ns/pF) C_L + 393 ns			15	115	400	1500	
Output Enable Delay from $\overline{CE}1$ or $\overline{CE}2$	5, 6	$t_{acc(\overline{CE}_n)}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Setup Time from A_n to $\overline{ST}$ or $\overline{CE}2$	4, 5, 6, 7	$t_{su(A)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	140	–	
Hold Time from A_n to $\overline{ST}$ or $\overline{CE}2$	4, 5, 6, 7	$t_{h(A)}$	5.0	600	200	–	ns
			10	240	80	–	
			15	180	55	–	
Data Hold Time	7	$t_{h(D)}$	5.0	1400	480	–	ns
			10	500	160	–	
			15	375	110	–	
Data Setup Time	7	$t_{su(D)}$	5.0	3600	1200	–	ns
			10	1800	600	–	
			15	1350	420	–	
Write Enable Hold Time	7	$t_{h(\overline{WE})}$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
Write Enable Setup Time	7	$t_{su(\overline{WE})}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Write Enable to D_{out} Disable**	4	$t_{\overline{WE}}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Strobe or $\overline{CE}2$ Pulse Width When Reading	4, 5, 6	$t_{WL(R)}$	5.0	1350	450	–	ns
			10	450	150	–	
			15	340	100	–	
Strobe, $\overline{CE}1$ or $\overline{CE}2$ Pulse Width When Writing	7	$t_{WL(W)}$	5.0	2400	1200	–	ns
			10	1260	600	–	
			15	945	420	–	
Write Recovery Time	4	$t_{R(W)}$					ns
t_W = (1.4 ns/pF) C_L + 219 ns			5.0	70	240	720	
t_W = (0.7 ns/pF) C_L + 70 ns			10	25	80	240	
t_W = (0.5 ns/pF) C_L + 47.5 ns			15	20	55	180	
$\overline{CE}1$ or $\overline{CE}2$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Read Setup Time	4, 5	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	4, 5	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Read Cycle Time	4, 5	$t_{cyc(R)}$	5.0	–	2500	6000	ns
			10	–	700	2100	
			15	–	500	1575	
Write Cycle Time	7	$t_{cyc(W)}$	5.0	–	1400	4800	ns
			10	–	700	2100	
			15	–	500	1575	

* The formula given is for the typical characteristics only.

** 10% output change into a 1.0 kΩ load.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT



Input	Output Source Characteristics	Output Sink Characteristics
$\overline{WE}$	Pulse Once	Pulse Once
D_{in}	SW1 in Position 1	SW1 in Position 2
V_{GS}	$-V_{DD}$	V_{DD}
V_{DS}	$V_{out} - V_{DD}$	V_{out}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

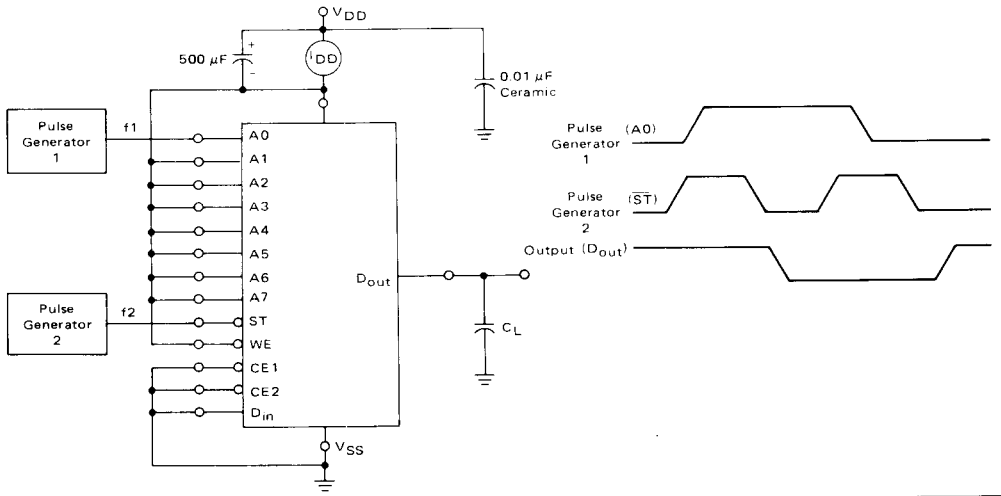


FIGURE 3 – AC TEST CIRCUIT

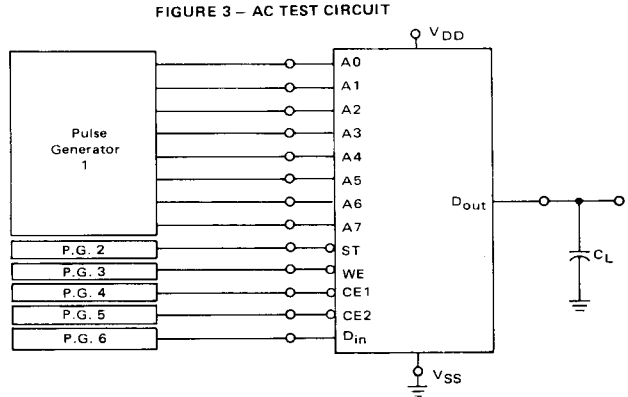
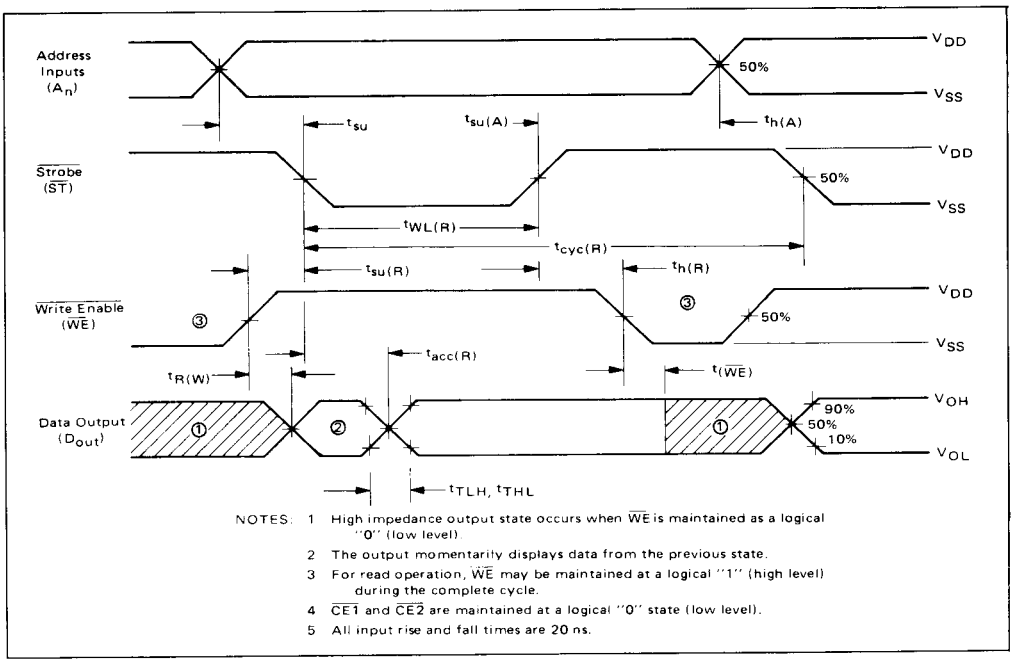
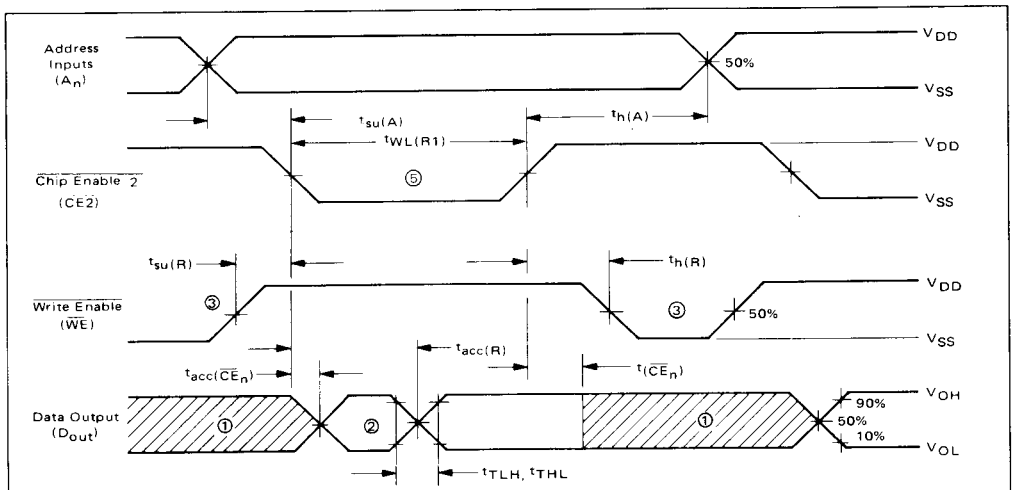


FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



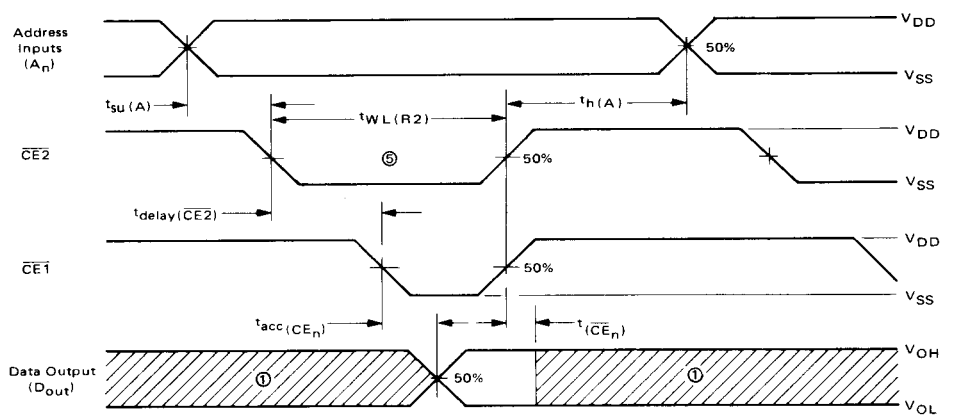
NOTES:
1. High impedance output state occurs when $\overline{WE}$ is maintained as a logical "0" (low level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. $\overline{CE1}$ and $\overline{CE2}$ are maintained at a logical "0" state (low level).
5. All input rise and fall times are 20 ns.

FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



NOTES:
1. High Impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. All input rise and fall times are 20 ns.
5. $t_{WL(R1)} \geq t_{acc}(R)$ max

FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY



NOTES: 1 High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).

2 $\overline{WE}$ is maintained at the logical "1" state for this example.

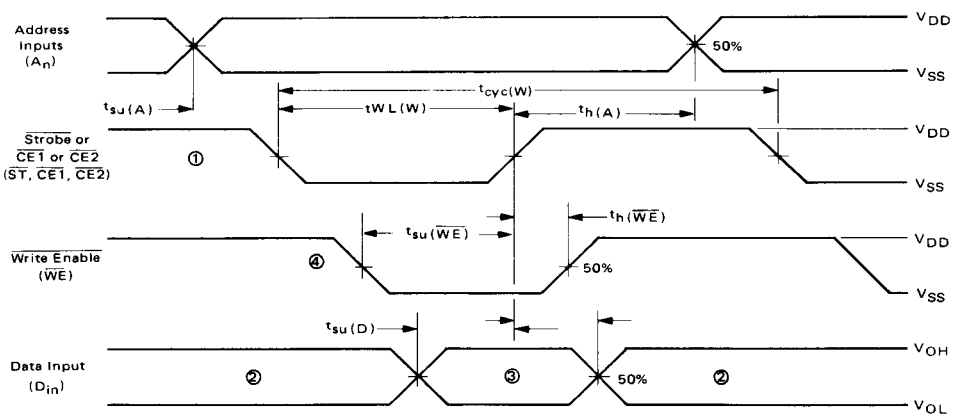
3 All input rise and fall times are 20 ns

4 $t_{delay(\overline{CE2})}$ minimum assuares that only data presently addressed will appear at the output.

$$t_{delay(\overline{CE2})\ min.} = t_{acc_{R\ max.}} - t_{acc(\overline{CE1})\ min.}$$

5 $t_{WL(R2)} \geqslant t_{delay\ (\overline{CE2})\ min} + t_{acc\ (CE_n)\ max}$

FIGURE 7 – WRITE CYCLE WAVEFORMS



NOTES: 1 The Strobe, $\overline{CE1}$ and $\overline{CE2}$ may be utilized to control a write cycle, however, during changes of address either Strobe or $\overline{CE2}$ must be in the logical "1" state (high level).

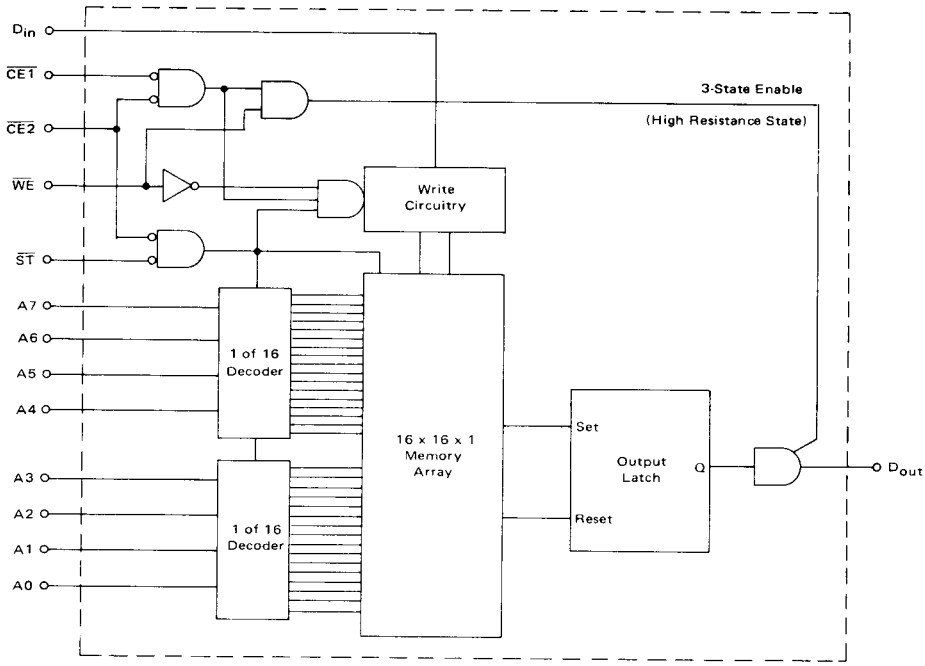
2 Data input logic level is don't care during the indicated intervals.

3 Data input logic level must remain fixed.

4 Write Enable may be maintained as a logical "0" during the write cycle.

5 All input rise and fall times are 20 ns.

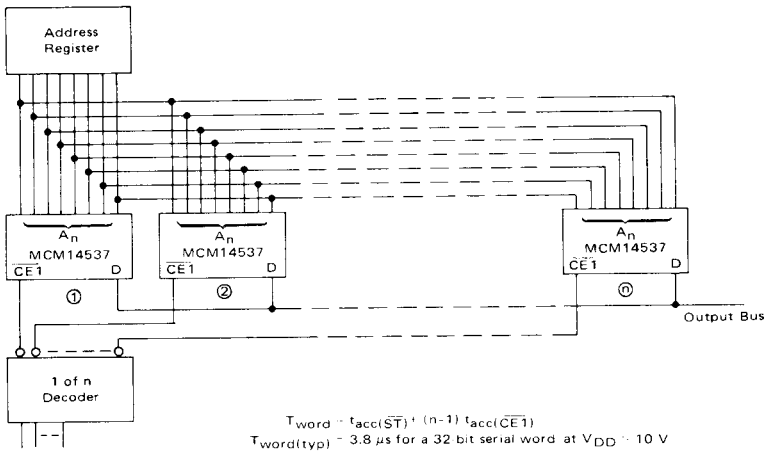
LOGIC/BLOCK DIAGRAM



FUNCTION	$\overline{CE1}$	$\overline{CE2}$	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D_{out} will be active if $\overline{CE1}$ and $\overline{CE2}$ = "0" and $\overline{WE}$ = "1".
	X	1	X	X	X	R	$\overline{CE2}$ = "1", fully disables internal logic and output.
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data.
D_{out} disabled in high resistance state	1	X	X	X	X	R	$\overline{CE1}$ = "1" disables write cycle and D_{out}.
	X	1	X	X	X	R	The chip is fully disabled.
	X	X	X	0	X	R	$\overline{WE}$ = "0" enables writing into memory if $\overline{CE1}$, $\overline{CE2}$, and $\overline{ST}$ = "0".
D_{out} enabled in active state	0	0	X	1	X	A	If $\overline{ST}$ = "1", the output stores and reads the previous data from or written into memory.
Read addressed memory location into output latch.	0	0	0	1	X	A	The output reads the present contents that are addressed.
	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take place in this condition.
	X	X	1	X	X	R/A	
Write into memory	0	0	0	0	A	R	D_{in} is written into memory and into the output latch
Write disabled	1	X	X	X	X	R	$\overline{WE}$ = "1" is a read enable.
	X	1	X	X	X	R	$\overline{WE}$ = "0" is a write enable.
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

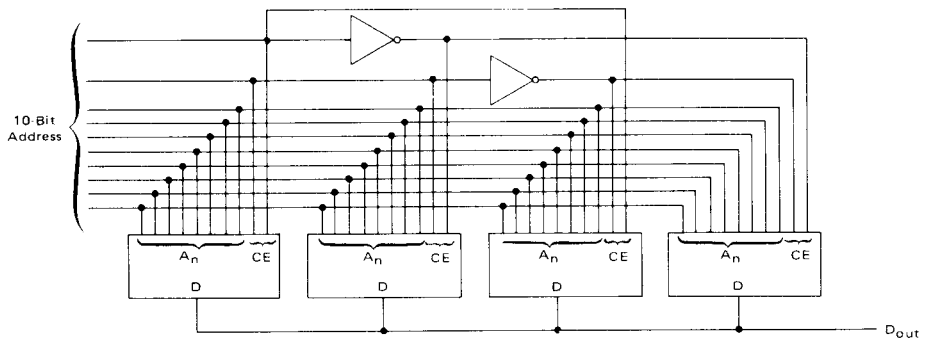
R = High resistance state at D_{out}
A = An active level of either V_{SS} or V_{DD}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES

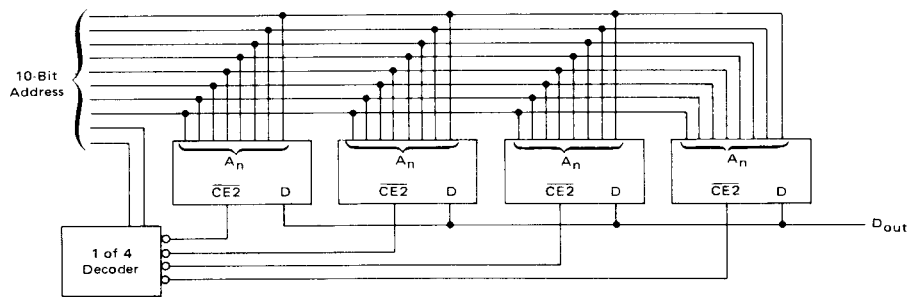


$T_{word} = t_{acc(\overline{ST})} + (n-1)\, t_{acc(\overline{CE1})}$

$T_{word(typ)} = 3.8\ \mu s$ for a 32 bit serial word at $V_{DD} = 10$ V



Typical 1024 x 1 RAM Utilizing Four MCM14537's.



Typical Low Power 1024 x 1 RAM Utilizing Four MCM14537's.