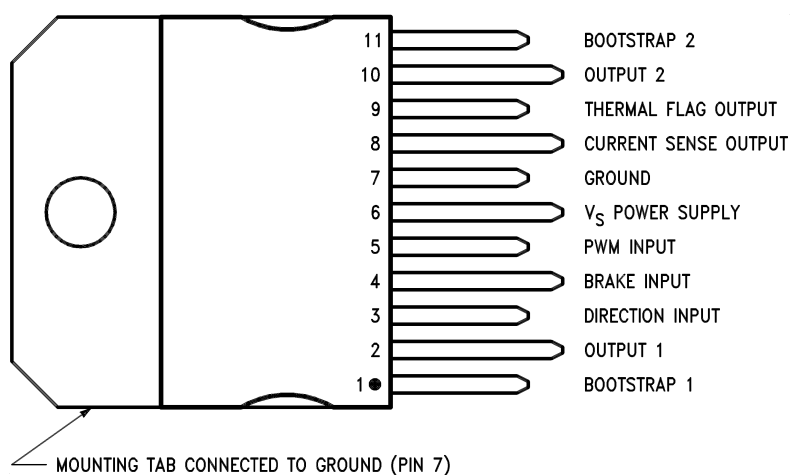




## Connection Diagram



**Figure 2. 11-Lead TO-220 Package  
Top View  
See Package NDJ0011B**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

Total Supply Voltage (V <sub>S</sub> , Pin 6)	60V
Voltage at Pins 3, 4, 5, 8 and 9	12V
Voltage at Bootstrap Pins (Pins 1 and 11)	V <sub>OUT</sub> +16V
Peak Output Current (200 ms)	6A
Continuous Output Current <sup>(3)</sup>	3A
Power Dissipation <sup>(4)</sup>	25W
Power Dissipation (T <sub>A</sub> = 25°C, Free Air)	3W
Junction Temperature, T <sub>J(max)</sub>	150°C
ESD Susceptibility <sup>(5)</sup>	1500V
Storage Temperature, T <sub>STG</sub>	–40°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) See [Application Information](#) for details regarding current limiting.
- (4) The maximum power dissipation must be derated at elevated temperatures and is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any temperature is P<sub>D(max)</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>, or the number given in the Absolute Ratings, whichever is lower. The typical thermal resistance from junction to case (θ<sub>JC</sub>) is 1.0°C/W and from junction to ambient (θ<sub>JA</sub>) is 30°C/W. For ensured operation T<sub>J(max)</sub> = 125°C.
- (5) Human-body model, 100 pF discharged through a 1.5 kΩ resistor. Except Bootstrap pins (pins 1 and 11) which are protected to 1000V of ESD.

## Operating Ratings<sup>(1)</sup>

Junction Temperature, T <sub>J</sub>	–40°C to +125°C
V <sub>S</sub> Supply Voltage	+12V to +55V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

## Electrical Characteristics<sup>(1)</sup>

The following specifications apply for V<sub>S</sub> = 42V, unless otherwise specified. **Boldface** limits apply over the entire operating temperature range, –40°C ≤ T<sub>J</sub> ≤ +125°C, all other limits are for T<sub>A</sub> = T<sub>J</sub> = 25°C.

Symbol	Parameter	Conditions	Typ	Limit	Units
R <sub>DS(ON)</sub>	Switch ON Resistance	Output Current = 3A <sup>(2)</sup>	0.33	0.40/ <b>0.6</b>	Ω (max)
R <sub>DS(ON)</sub>	Switch ON Resistance	Output Current = 6A <sup>(2)</sup>	0.38	0.45/ <b>0.6</b>	Ω (max)
V <sub>CLAMP</sub>	Clamp Diode Forward Drop	Clamp Current = 3A <sup>(2)</sup>	1.2	1.5	V (max)
V <sub>IL</sub>	Logic Low Input Voltage	Pins 3, 4, 5		<b>–0.1</b> <b>0.8</b>	V (min) V (max)
I <sub>IL</sub>	Logic Low Input Current	V <sub>IN</sub> = –0.1V, Pins = 3, 4, 5		<b>–10</b>	μA (max)
V <sub>IH</sub>	Logic High Input Voltage	Pins 3, 4, 5		<b>2</b> <b>12</b>	V (min) V (max)
I <sub>IH</sub>	Logic High Input Current	V <sub>IN</sub> = 12V, Pins = 3, 4, 5		<b>10</b>	μA (max)
	Current Sense Output	I <sub>OUT</sub> = 1A <sup>(3)</sup>	377	325/ <b>300</b> 425/ <b>450</b>	μA (min) μA (max)
	Current Sense Linearity	1A ≤ I <sub>OUT</sub> ≤ 3A <sup>(4)</sup>	±6	±9	%

- (1) All limits are 100% production tested at 25°C. Temperature extreme limits are ensured via correlation using accepted SQC (Statistical Quality Control) methods. All limits are used to calculate AOQL, (Average Outgoing Quality Level).
- (2) Output currents are pulsed (t<sub>W</sub> < 2 ms, Duty Cycle < 5%).
- (3) Selections for tighter tolerance are available. Contact factory.
- (4) Regulation is calculated relative to the current sense output value with a 1A load.

## Electrical Characteristics <sup>(1)</sup> (continued)

The following specifications apply for  $V_S = 42V$ , unless otherwise specified. **Boldface** limits apply over the entire operating temperature range,  $-40^{\circ}C \leq T_J \leq +125^{\circ}C$ , all other limits are for  $T_A = T_J = 25^{\circ}C$ .

Symbol	Parameter	Conditions	Typ	Limit	Units
	Undervoltage Lockout	Outputs turn OFF		9 11	V (min) V (max)
$T_{JW}$	Warning Flag Temperature	Pin 9 $\leq 0.8V$ , $I_L = 2\text{ mA}$	145		$^{\circ}C$
$V_F(ON)$	Flag Output Saturation Voltage	$T_J = T_{JW}$ , $I_L = 2\text{ mA}$	0.15		V
$I_F(OFF)$	Flag Output Leakage	$V_F = 12V$	0.2	10	$\mu A$ (max)
$T_{JSD}$	Shutdown Temperature	Outputs Turn OFF	170		$^{\circ}C$
$I_S$	Quiescent Supply Current	All Logic Inputs Low	13	25	mA (max)
$t_{Don}$	Output Turn-On Delay Time	Sourcing Outputs, $I_{OUT} = 3A$ Sinking Outputs, $I_{OUT} = 3A$	300 300		ns ns
$t_{on}$	Output Turn-On Switching Time	Bootstrap Capacitor = 10 nF Sourcing Outputs, $I_{OUT} = 3A$ Sinking Outputs, $I_{OUT} = 3A$	100 80		ns ns
$t_{Doff}$	Output Turn-Off Delay Times	Sourcing Outputs, $I_{OUT} = 3A$ Sinking Outputs, $I_{OUT} = 3A$	200 200		ns ns
$t_{off}$	Output Turn-Off Switching Times	Bootstrap Capacitor = 10 nF Sourcing Outputs, $I_{OUT} = 3A$ Sinking Outputs, $I_{OUT} = 3A$	75 70		ns ns
$t_{pw}$	Minimum Input Pulse Width	Pins 3, 4 and 5	1		$\mu s$
$t_{cpr}$	Charge Pump Rise Time	No Bootstrap Capacitor	20		$\mu s$

## Typical Performance Characteristics

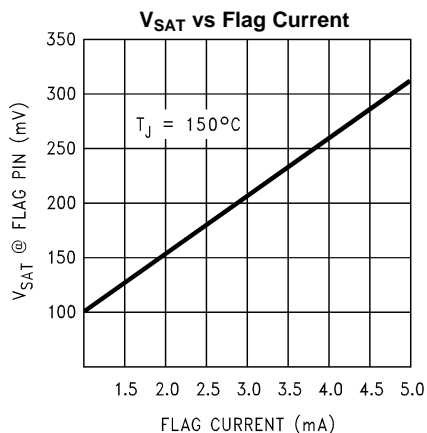


Figure 3.

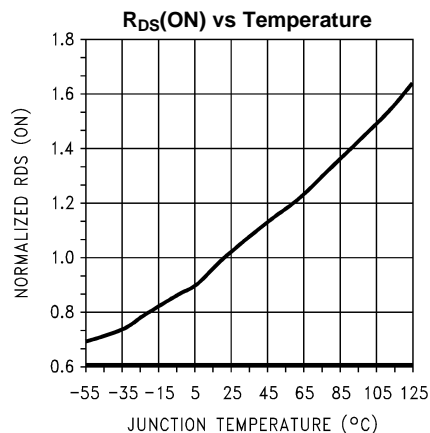


Figure 4.

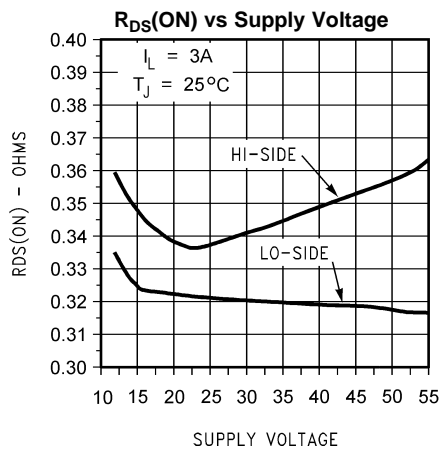


Figure 5.

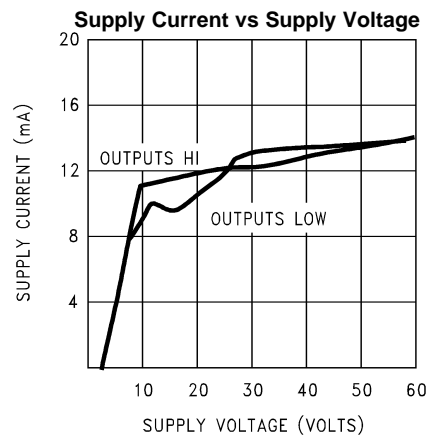


Figure 6.

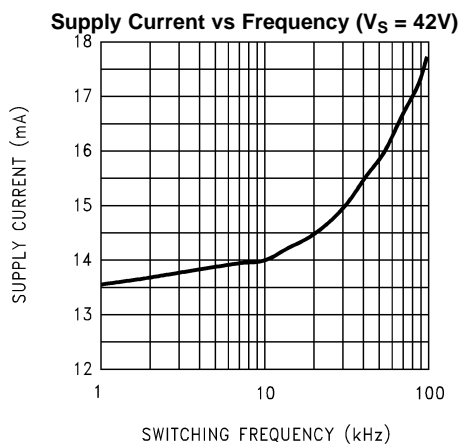


Figure 7.

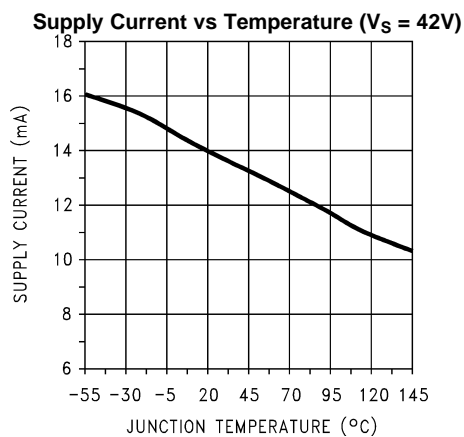


Figure 8.

## Typical Performance Characteristics (continued)

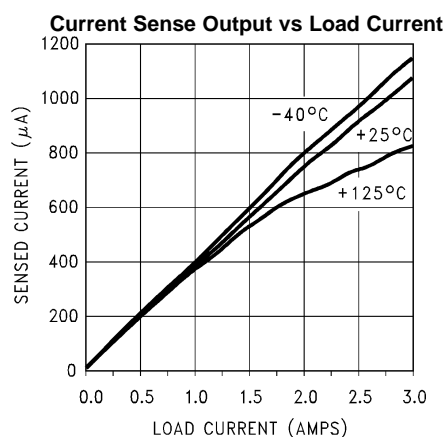


Figure 9.

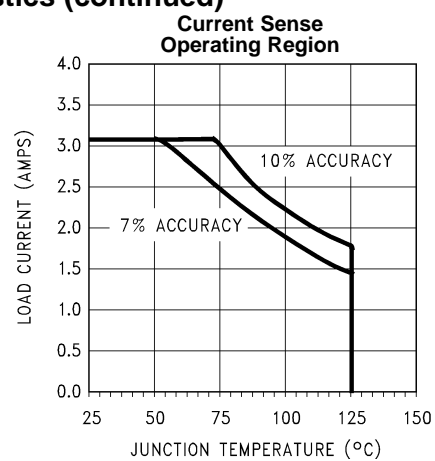
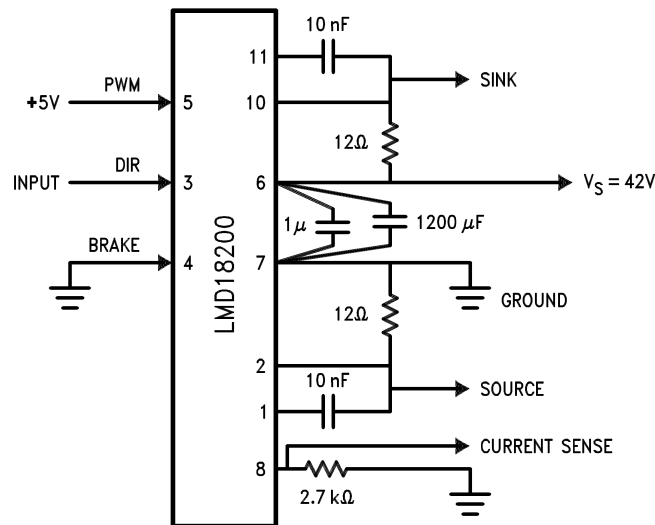
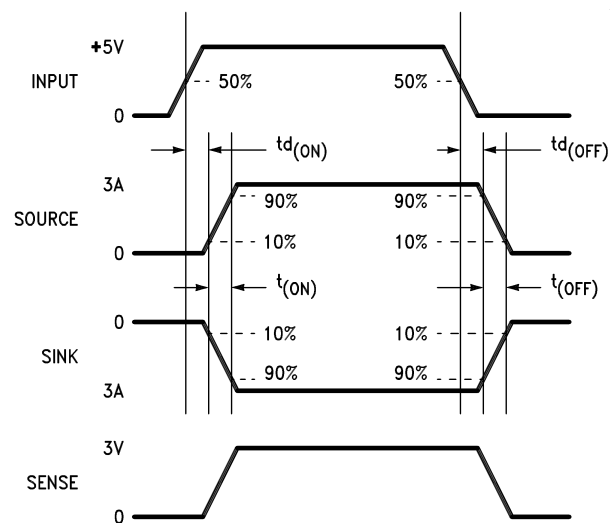


Figure 10.

## TEST CIRCUIT



## Switching Time Definitions



## Pinout Description

(See [Test Circuit](#))

**Pin 1, BOOTSTRAP 1 Input:** Bootstrap capacitor pin for half H-bridge number 1. The recommended capacitor (10 nF) is connected between pins 1 and 2.

**Pin 2, OUTPUT 1:** Half H-bridge number 1 output.

**Pin 3, DIRECTION Input:** See [Logic Truth Table](#). This input controls the direction of current flow between OUTPUT 1 and OUTPUT 2 (pins 2 and 10) and, therefore, the direction of rotation of a motor load.

**Pin 4, BRAKE Input:** See [Logic Truth Table](#). This input is used to brake a motor by effectively shorting its terminals. When braking is desired, this input is taken to a logic high level and it is also necessary to apply logic high to PWM input, pin 5. The drivers that short the motor are determined by the logic level at the DIRECTION input (Pin 3): with Pin 3 logic high, both current sourcing output transistors are ON; with Pin 3 logic low, both current sinking output transistors are ON. All output transistors can be turned OFF by applying a logic high to Pin 4 and a logic low to PWM input Pin 5; in this case only a small bias current (approximately  $-1.5\text{ mA}$ ) exists at each output pin.

**Pin 5, PWM Input:** See [Logic Truth Table](#). How this input (and DIRECTION input, Pin 3) is used is determined by the format of the PWM Signal.

**Pin 6,  $V_S$  Power Supply**

**Pin 7, GROUND Connection:** This pin is the ground return, and is internally connected to the mounting tab.

**Pin 8, CURRENT SENSE Output:** This pin provides the sourcing current sensing output signal, which is typically  $377\text{ }\mu\text{A/A}$ .

**Pin 9, THERMAL FLAG Output:** This pin provides the thermal warning flag output signal. Pin 9 becomes active-low at  $145^\circ\text{C}$  (junction temperature). However the chip will not shut itself down until  $170^\circ\text{C}$  is reached at the junction.

**Pin 10, OUTPUT 2:** Half H-bridge number 2 output.

**Pin 11, BOOTSTRAP 2 Input:** Bootstrap capacitor pin for Half H-bridge number 2. The recommended capacitor (10 nF) is connected between pins 10 and 11.

**Logic Truth Table**

PWM	Dir	Brake	Active Output Drivers
H	H	L	Source 1, Sink 2
H	L	L	Sink 1, Source 2
L	X	L	Source 1, Source 2
H	H	H	Source 1, Source 2
H	L	H	Sink 1, Sink 2
L	X	H	NONE



## APPLICATION INFORMATION

### TYPES OF PWM SIGNALS

The LMD18200 readily interfaces with different forms of PWM signals. Use of the part with two of the more popular forms of PWM is described in the following paragraphs.

**Simple, locked anti-phase PWM** consists of a single, variable duty-cycle signal in which is encoded both direction and amplitude information (see [Figure 11](#)). A 50% duty-cycle PWM signal represents zero drive, since the net value of voltage (integrated over one period) delivered to the load is zero. For the LMD18200, the PWM signal drives the direction input (pin 3) and the PWM input (pin 5) is tied to logic high.

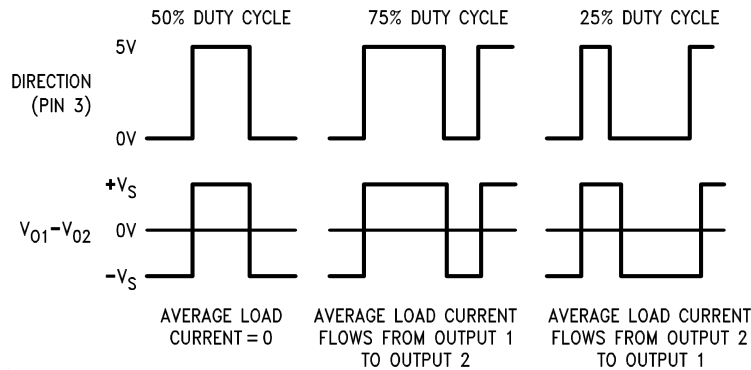


Figure 11. Locked Anti-Phase PWM Control

**Sign/magnitude PWM** consists of separate direction (sign) and amplitude (magnitude) signals (see [Figure 12](#)). The (absolute) magnitude signal is duty-cycle modulated, and the absence of a pulse signal (a continuous logic low level) represents zero drive. Current delivered to the load is proportional to pulse width. For the LMD18200, the DIRECTION input (pin 3) is driven by the sign signal and the PWM input (pin 5) is driven by the magnitude signal.

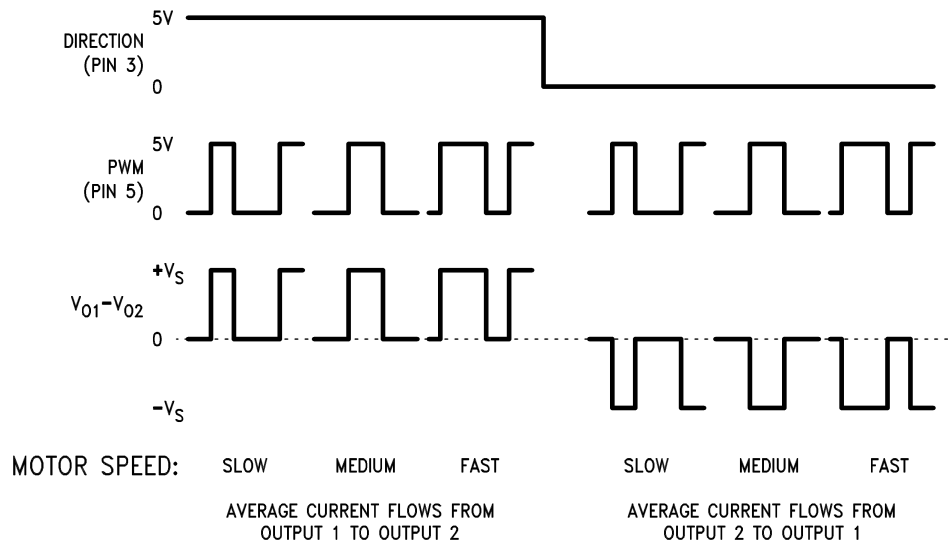
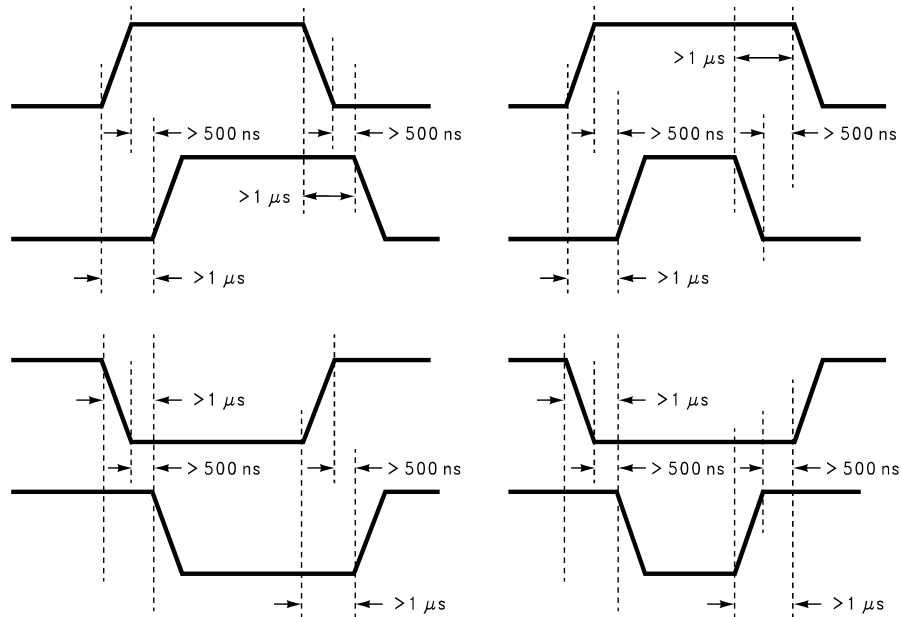


Figure 12. Sign/Magnitude PWM Control

### SIGNAL TRANSITION REQUIREMENTS

To ensure proper internal logic performance, it is good practice to avoid aligning the falling and rising edges of input signals. A delay of at least 1  $\mu$ sec should be incorporated between transitions of the Direction, Brake, and/or PWM input signals. A conservative approach is be sure there is at least 500ns delay between the end of the first transition and the beginning of the second transition. See [Figure 13](#).



**Figure 13. Transitions in Brake, Direction, or PWM Must Be Separated By At Least 1 μsec**

## USING THE CURRENT SENSE OUTPUT

The CURRENT SENSE output (pin 8) has a sensitivity of 377  $\mu\text{A}$  per ampere of output current. For optimal accuracy and linearity of this signal, the value of voltage generating resistor between pin 8 and ground should be chosen to limit the maximum voltage developed at pin 8 to 5V, or less. The maximum voltage compliance is 12V.

It should be noted that the recirculating currents (free wheeling currents) are ignored by the current sense circuitry. Therefore, only the currents in the upper sourcing outputs are sensed.

## USING THE THERMAL WARNING FLAG

The THERMAL FLAG output (pin 9) is an open collector transistor. This permits a wired OR connection of thermal warning flag outputs from multiple LMD18200's, and allows the user to set the logic high level of the output signal swing to match system requirements. This output typically drives the interrupt input of a system controller. The interrupt service routine would then be designed to take appropriate steps, such as reducing load currents or initiating an orderly system shutdown. The maximum voltage compliance on the flag pin is 12V.

## SUPPLY BYPASSING

During switching transitions the levels of fast current changes experienced may cause troublesome voltage transients across system stray inductance.

It is normally necessary to bypass the supply rail with a high quality capacitor(s) connected as close as possible to the  $V_S$  Power Supply (Pin 6) and GROUND (Pin 7). A 1  $\mu\text{F}$  high-frequency ceramic capacitor is recommended. Care should be taken to limit the transients on the supply pin below the Absolute Maximum Rating of the device. When operating the chip at supply voltages above 40V a voltage suppressor (transorb) such as P6KE62A is recommended from supply to ground. Typically the ceramic capacitor can be eliminated in the presence of the voltage suppressor. Note that when driving high load currents a greater amount of supply bypass capacitance (in general at least 100  $\mu\text{F}$  per Amp of load current) is required to absorb the recirculating currents of the inductive loads.

## CURRENT LIMITING

Current limiting protection circuitry has been incorporated into the design of the LMD18200. With any power device it is important to consider the effects of the substantial surge currents through the device that may occur as a result of shorted loads. The protection circuitry monitors this increase in current (the threshold is set to approximately 10 Amps) and shuts off the power device as quickly as possible in the event of an overload condition. In a typical motor driving application the most common overload faults are caused by shorted motor windings and locked rotors. Under these conditions the inductance of the motor (as well as any series inductance in the  $V_{CC}$  supply line) serves to reduce the magnitude of a current surge to a safe level for the LMD18200. Once the device is shut down, the control circuitry will periodically try to turn the power device back on. This feature allows the immediate return to normal operation in the event that the fault condition has been removed. While the fault remains however, the device will cycle in and out of thermal shutdown. This can create voltage transients on the  $V_{CC}$  supply line and therefore proper supply bypassing techniques are required.

The most severe condition for any power device is a direct, hard-wired (“screwdriver”) long term short from an output to ground. This condition can generate a surge of current through the power device on the order of 15 Amps and require the die and package to dissipate up to 500 Watts of power for the short time required for the protection circuitry to shut off the power device. This energy can be destructive, particularly at higher operating voltages (>30V) so some precautions are in order. Proper heat sink design is essential and it is normally necessary to heat sink the  $V_{CC}$  supply pin (pin 6) with 1 square inch of copper on the PCB.

## INTERNAL CHARGE PUMP AND USE OF BOOTSTRAP CAPACITORS

To turn on the high-side (sourcing) DMOS power devices, the gate of each device must be driven approximately 8V more positive than the supply voltage. To achieve this an internal charge pump is used to provide the gate drive voltage. As shown in Figure 14, an internal capacitor is alternately switched to ground and charged to about 14V, then switched to  $V$  supply thereby providing a gate drive voltage greater than  $V$  supply. This switching action is controlled by a continuously running internal 300 kHz oscillator. The rise time of this drive voltage is typically 20  $\mu$ s which is suitable for operating frequencies up to 1 kHz.

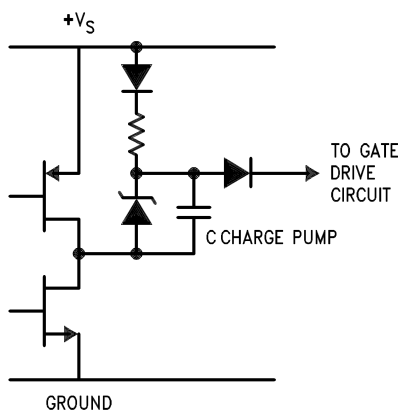


Figure 14. Internal Charge Pump Circuitry

For higher switching frequencies, the LMD18200 provides for the use of external bootstrap capacitors. The bootstrap principle is in essence a second charge pump whereby a large value capacitor is used which has enough energy to quickly charge the parasitic gate input capacitance of the power device resulting in much faster rise times. The switching action is accomplished by the power switches themselves Figure 15. External 10 nF capacitors, connected from the outputs to the bootstrap pins of each high-side switch provide typically less than 100 ns rise times allowing switching frequencies up to 500 kHz.

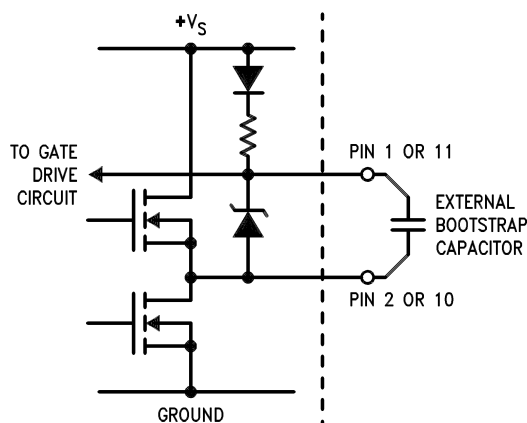


Figure 15. Bootstrap Circuitry

## INTERNAL PROTECTION DIODES

A major consideration when switching current through inductive loads is protection of the switching power devices from the large voltage transients that occur. Each of the four switches in the LMD18200 have a built-in protection diode to clamp transient voltages exceeding the positive supply or ground to a safe diode voltage drop across the switch.

The reverse recovery characteristics of these diodes, once the transient has subsided, is important. These diodes must come out of conduction quickly and the power switches must be able to conduct the additional reverse recovery current of the diodes. The reverse recovery time of the diodes protecting the sourcing power devices is typically only 70 ns with a reverse recovery current of 1A when tested with a full 6A of forward current through the diode. For the sinking devices the recovery time is typically 100 ns with 4A of reverse current under the same conditions.

## TYPICAL APPLICATIONS

### FIXED OFF-TIME CONTROL

This circuit controls the current through the motor by applying an average voltage equal to zero to the motor terminals for a fixed period of time, whenever the current through the motor exceeds the commanded current. This action causes the motor current to vary slightly about an externally controlled average level. The duration of the Off-period is adjusted by the resistor and capacitor combination of the LM555. In this circuit the Sign/Magnitude mode of operation is implemented (see [TYPES OF PWM SIGNALS](#)).

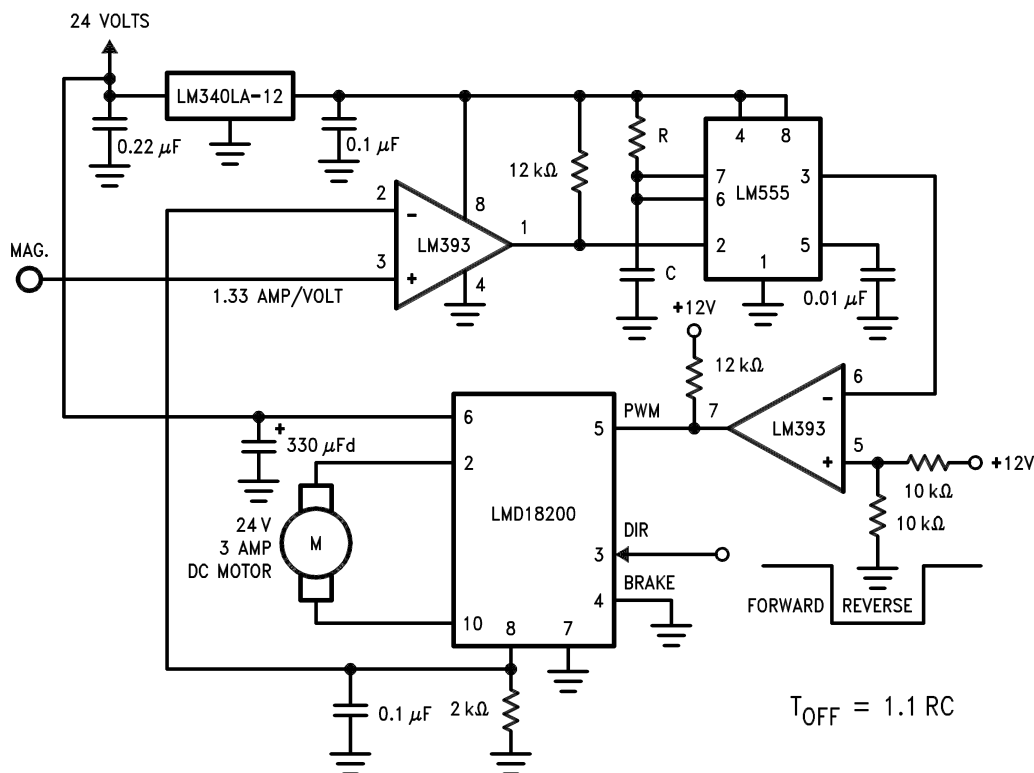


Figure 16. Fixed Off-Time Control

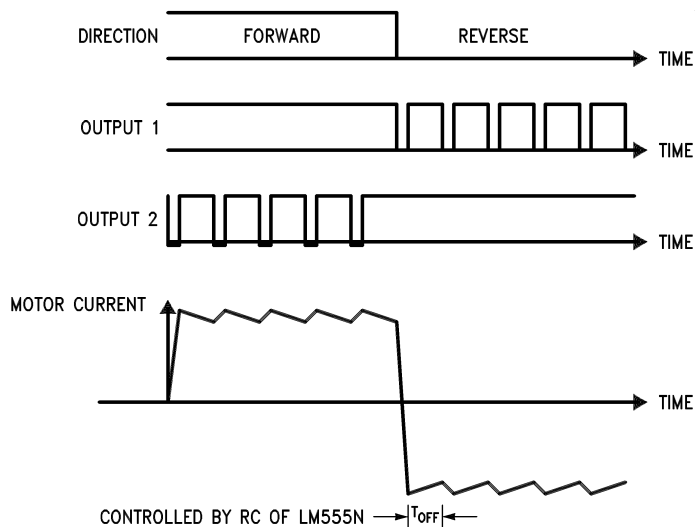


Figure 17. Switching Waveforms

## TORQUE REGULATION

Locked Anti-Phase Control of a brushed DC motor. Current sense output of the LMD18200 provides load sensing. The LM3524D is a general purpose PWM controller. The relationship of peak motor current to adjustment voltage is shown in Figure 19.

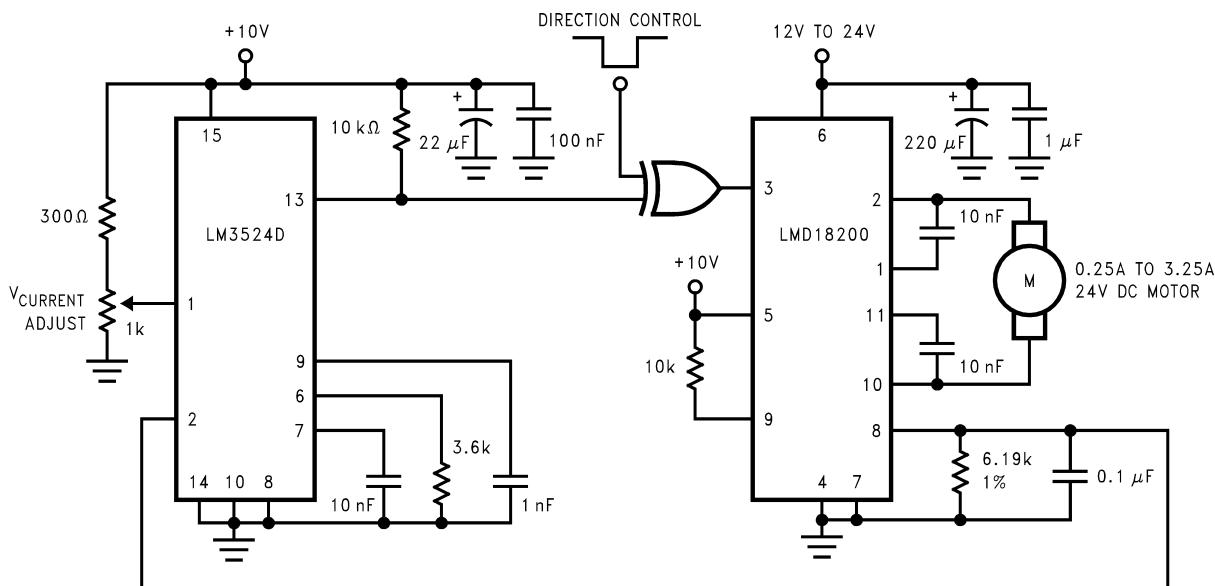


Figure 18. Locked Anti-Phase Control Regulates Torque

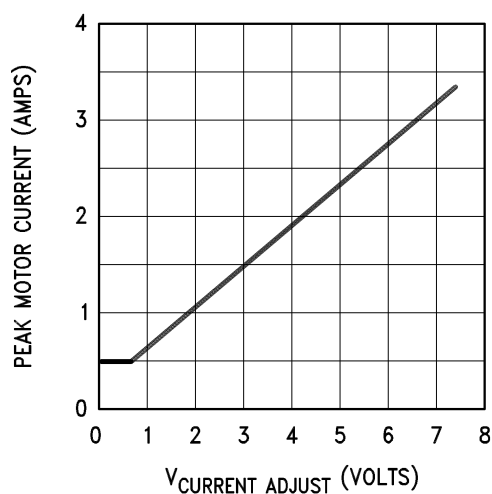


Figure 19. Peak Motor Current vs Adjustment Voltage

## VELOCITY REGULATION

Utilizes tachometer output from the motor to sense motor speed for a locked anti-phase control loop. The relationship of motor speed to the speed adjustment control voltage is shown in Figure 21.

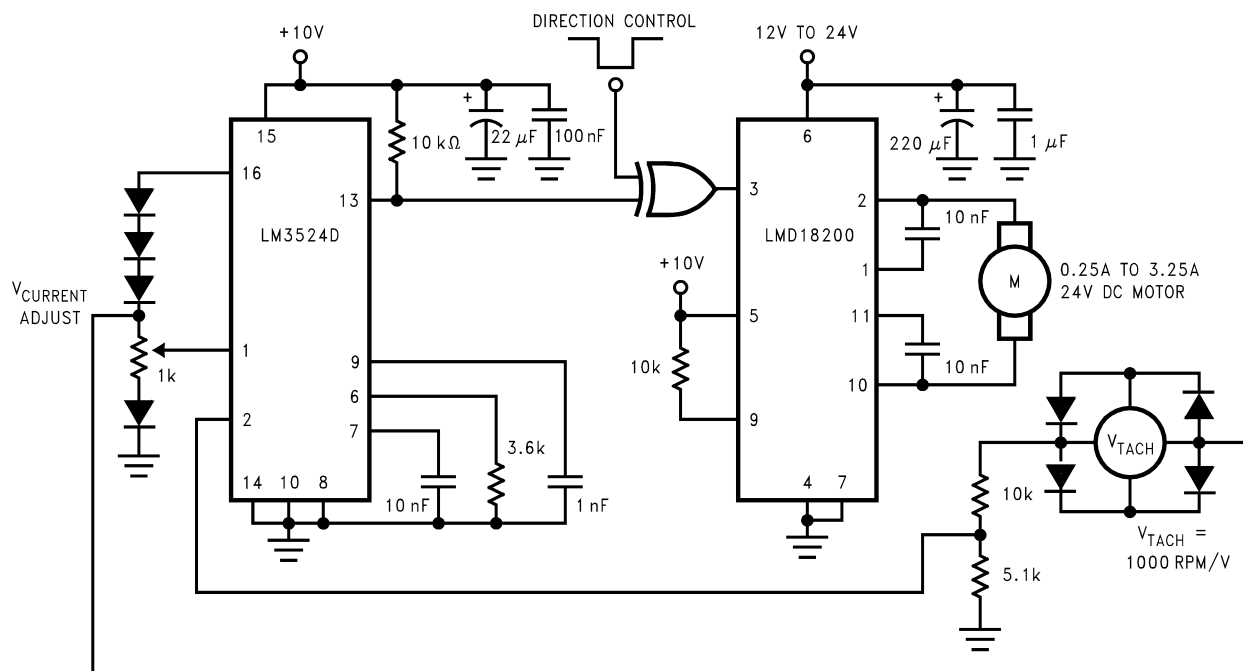


Figure 20. Regulate Velocity with Tachometer Feedback

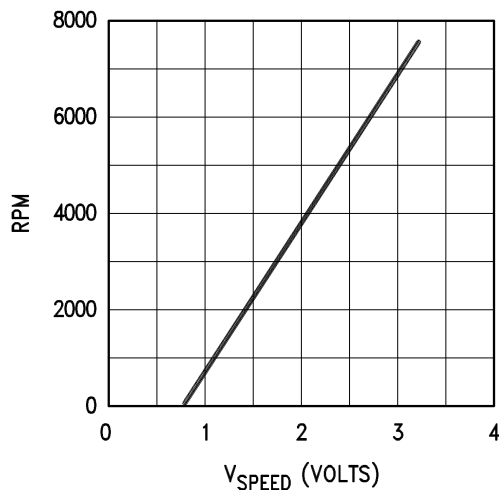


Figure 21. Motor Speed vs Control Voltage

## REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
<ul style="list-style-type: none"><li>Changed layout of National Data Sheet to TI format .....</li></ul>	<a href="#">15</a>



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMD18200T	NRND	TO-220	NDJ	11	20	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 125	LMD18200T P+	
LMD18200T/LF14	ACTIVE	TO-220	NDJ	11	23	RoHS & Green	SN	Level-1-NA-UNLIM		LMD18200T P+	<a href="#">Samples</a>
LMD18200T/NOPB	ACTIVE	TO-220	NDJ	11	20	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LMD18200T P+	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

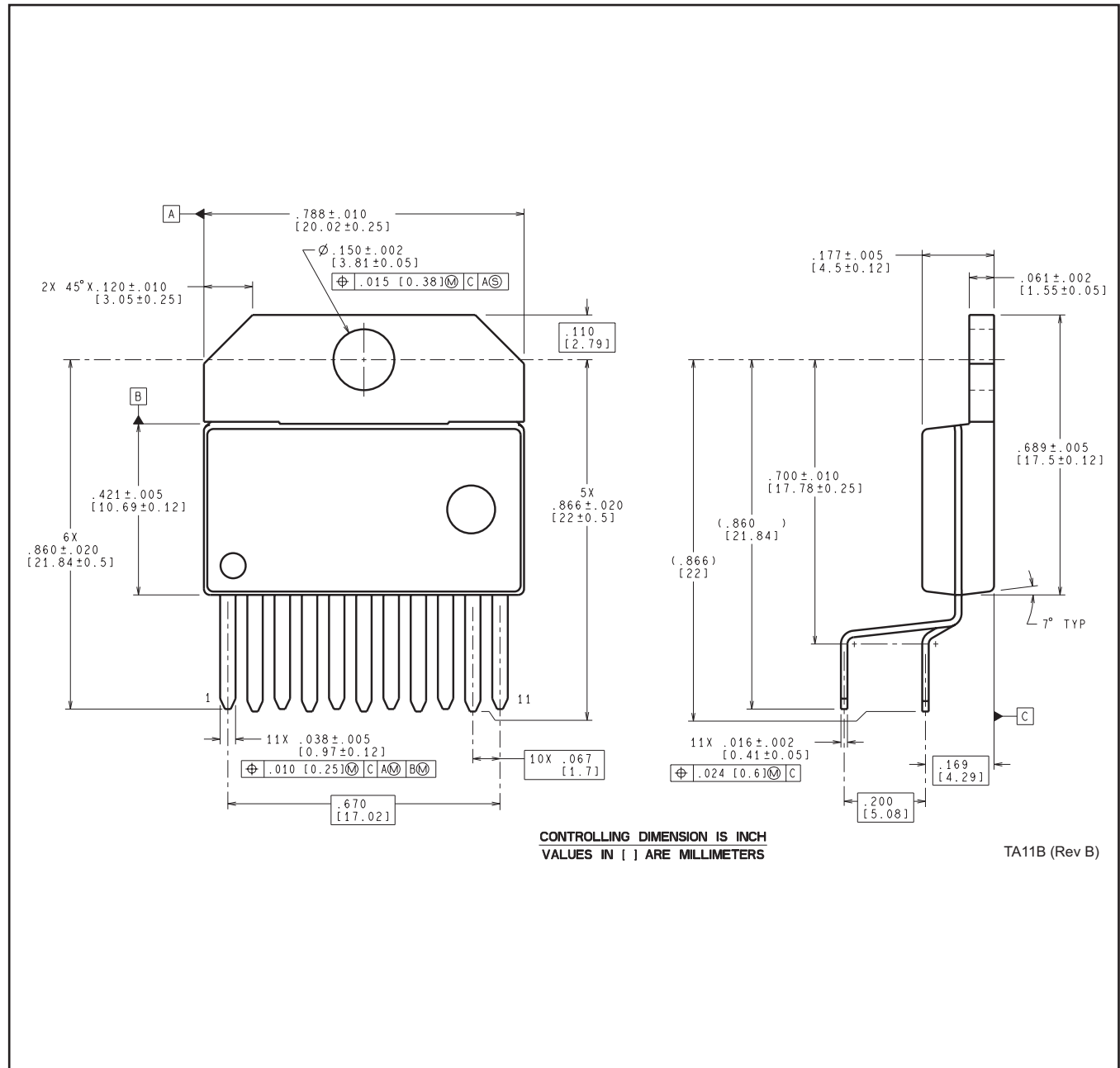
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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