Ordering number : ENA0069

SANYO Semiconductors
DATA SHEET

LA76832N — Monolithic Linear IC
I²C Bus Control IC

Overview

The LA76832N is I²C bus controller ICs that support the NTSC and aim for rationalization of color TV set design, improved manufacturability, and lower total costs.

Functions

- I²C Bus Control VIF/SIF/Y/C/Deflection Implemented in a Single Chip

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_8 max		7.0	V
	V_{31} max		7.0	V
	V_{43} max		7.0	V
Maximum supply current	I_{18} max		25	mA
	I_{25} max		35	mA
Allowable power dissipation	Pd max	Ta≤65°C *	1.6	W
Operating temperature	Topr		-10 to +65	°C
Storage temperature	Tstg		-55 to +150	°C

*Provided with a glass epoxy board (114.3×76.1×1.6mm)

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_8		5.0	V
	V_{31}		5.0	V
	V_{43}		5.0	V
Recommended supply current	I_{18}		19	mA
	I_{25}		27	mA
Operating supply voltage range	V_8 op		4.7 to 5.3	V
	V_{31} op		4.7 to 5.3	V
	V_{43} op		4.7 to 5.3	V
Operating supply current range	I_{25} op		24 to 30	mA
	I_{18} op		17 to 21	mA

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Electrical Characteristics at Ta = 25°C, $V_{CC}L = V_8 = V_{31} = V_{43} = 5.0V$, $I_{CC} = I_{18} = 19mA$, $I_{CC} = I_{25} = 27mA$

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
[Circuit voltage, current]							
IF supply current		I_8	V_8 = 5V V_3 = 2.5V	55.0	65.0	75.0	mA
RGB supply current		V_{18}	I_{18} = 19mA		8.0		V
Horizontal supply voltage		V_{25}	I_{25} = 27mA		5.0		V
CCD supply current		I_{31}	I_{31} = 5V		5.6		mA
Video supply current		I_{43}	I_{43} = 5V		150		mA
[CCD block]							
Voltage gain		G_{V_R}		-2	0	+2	dB
Voltage gain B		G_{V_B}		-2	0	+2	dB
Difference of voltage gain		D_{GV}		0	0.1	0.3	dB
Delay time		Td			63.8		µs
[OSD block]							
OSD Fast SW threshold		FSTH		2.3	2.5	2.7	V
Red RGB output level		$R_{OSD}H$		120	165	200	IRE
Green RGB output level		$G_{OSD}H$		70	120	140	IRE
Blue RGB output level		$B_{OSD}H$		85	120	155	IRE
Analog OSD R output level	Gain match	R_{RGB}		1.12	1.4	1.68	Ratio
	Linearity	LR_{RGB}		45	50	60	%
Analog OSD G output level	Gain match	G_{RGB}		0.8	1.0	1.2	Ratio
	Linearity	LG_{RGB}		45	50	60	%
Analog OSD B output level	Gain Match	B_{RGB}		0.8	1.0	1.2	Ratio
	Linearity	LB_{RGB}		45	50	60	%
[RGB output (cutoff drive) block]							
Brightness control	(Normal)	BRT63		1.9	2.2	2.5	V
	Hi brightness (max)	BRT127			40		IRE
	Low brightness (Min)	BRT0			40		IRE
Cutoff control (min)		$V_{bias}0$		1.6	2.0	2.4	V
(Bias control) (max)		$V_{bias}255$		2.8	3.2	3.6	V
Resolution		$V_{bias}sns$			4		mV/Bit
Sub-bias control Resolution		$Vs_{bias}sns$			8		mV/Bit
RB Drive adjustment Maximum output		$RB_{out}127$			2.7		Vp-p
G Drive adjustment Maximum output		$G_{out}15$			1.8		Vp-p
RB Output attenuation		$RB_{out}0$		7	9	11	dB
G Output attenuation		$G_{out}0$		1.5	3.5	5.5	dB
[VIF block]							
Maximum RFAGC voltage		$V_{RF}H$	CW = 80dBµ, DAC = 0	8.5	9		Vdc
Minimum RFAGC voltage		$V_{RF}L$	CW = 80dBµ, DAC = 63	0	0.3	0.7	Vdc
RF AGC Delay Pt (@DAC = 0)		$RF_{AGC}0$	DAC = 0	85			dBµ
RF AGC Delay Pt (@DAC = 63)		$RF_{AGC}63$	DAC = 63			75	dBµ
Input sensitivity		V_i	Output -3dB			46	dBµ
No-signal video output voltage		VOn	No signal	3.3	3.7	4.1	Vdc
Sync signal tip level		VOtip	CW = 80dBµ	1.1	1.4	1.7	Vdc
Video output amplitude		VO	80dBµ, AM = 78%, fm = 15kHz	1.9	2.0	2.1	Vp-p
Video S/N		S/N	CW = 80dBµ		45		dB
C-S beat level		IC-S	V3.58MHz/V920MHz		30		dB
Differential gain		D_G	80dBµ, 87.5% Video MOD		5.0	10.0	%
Differential phase		D_P	80dBµ, 87.5% Video MOD		2.0	10.0	deg
Maximum AFT output voltage		$V_{AFT}H$	CW = 80dBµ, frequency variations	4.3	4.7	5.0	Vdc
Minimum AFT output voltage		$V_{AFT}L$	CW = 80dBµ, frequency variations	0.0	0.2	0.7	Vdc
AFT detection sensitivity		$V_{AFT}S$	CW = 80dBµ, frequency variations	12.0	20.0	28.0	mV/kHz

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Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
APC pull-in range (U)		f_PU		1.0			MHz
APC pull-in range (L)		f_PL		1.0			MHz
[SIF block]							
FM detection output voltage		SO_{ADJ}			500		mVrms
FM limiting sensitivity		SL_S	Output -3dB			61	dBμ
FM detection output f characteristics		S_F	fm = 100kHz	-0.5	6.0	9.0	dB
FM detection output distortion		S_{THD}	FM = ±25kHz			1.0	%
AM rejection ratio		S_{AMR}	AM = 30%	40			dB
SIF S/N		S_{SN}	DIN. Andio	50			dB
de-emph time constant		S_{NTC}			3.0		dB
[AUDIO block]							
Maximum gain		AG_{MAX}	1kHz	-2.5	0.0	+2.5	dB
Variable range		A_{RANGE}		60	65		dB
Frequency characteristics		A_F	20kHz	-3.0	0.0	+3.0	dB
Mute		A_{MUTE}	20kHz	70			dB
Distortion		A_{THD}	1kHz, 500mVrms, Vol : MAX			0.5	%
S/N		A_{SN}	DIN. Audio	65	70		dB
Crosstalk		A_{CT}	1kHz	70			dB
[Video SW block]							
Video signal input 1DC voltage		$V_{IN}1_{DC}$		2.2	2.5	2.8	V
Video signal input 1AC voltage		$V_{IN}1_{AC}$			1		Vp-p
Video signal input 2DC voltage		$V_{IN}2_{DC}$		2.2	2.5	2.8	V
Video signal input 2AC voltage		$V_{IN}2_{AC}$			1		Vp-p
SVO terminal DC voltage		SVO_{DC}		1.7	2.0	2.3	V
SVO terminal AC voltage		SVO_{AC}		1.7	2.0	2.3	Vp-p
[Filter block]							
Chroma trap amount NTSC		C_{trap}N		-36.0	-26.0	-22.0	dB
Chroma trap amount PAL		C_{trap}P		-36.0	-26.0	-22.0	dB
C-BPF1A (3.93MHz)		C_{BPF}1A	Reference : 4.43MHz FILTER SYS = 0010	-6.0	-3.0	0.0	dB
C-BPF1B (4.73/4.13MHz)		C_{BPF}1B	Reference : 4.13MHz FILTER SYS = 0010	-0.5	1.5	3.5	dB
C-BPF1C (4.93/3.93MHz)		C_{BPF}1C	Reference : 3.93MHz FILTER SYS = 0010	6.0	4.0	1.0	dB
C-BPF2A (3.93MHz)		C_{BPF}2A	Reference : 4.43MHz FILTER SYS = 0011	-4.0	-1.0	0.0	dB
C-BPF2B (4.73/4.13MHz)		C_{BPF}2B	Reference : 4.13MHz FILTER SYS = 0011	-2.0	0.0	2.0	dB
C-BPF2C (4.93/3.93MHz)		C_{BPF}2C	Reference : 3.93MHz FILTER SYS = 0011	-2.5	0.0	2.5	dB
Y-DL TIME1 6MHz Trap		T_dY1	FILTER SYS = 0100	300.0	350.0	400.0	ns
Y-DL TIME2 PAL		T_dY2	FILTER SYS = 0010	490.0	540.0	590.0	ns
Y-DL TIME3 NTSC		T_dY3	FILTER SYS = 0001	530.0	580.0	630.0	ns
[Video block]							
Video overall gain (Contrast max)		CONT127		9.0	11.0	13.0	dB
Contrast adjustment characteristics (Normal/max)		CONT63		-7.5	-6.0	-4.5	dB
Contrast adjustment characteristics (Min/max)		CONT0		-15.0	-12.0	-9.0	dB
Sharpness variability range	(Normal)	Sharp31	FILTER SYS = 0000	6.0	9.0	12.0	dB
	(max)	Sharp63	FILTER SYS = 0000	9.0	12.0	15.0	dB
	(min)	Sharp0	FILTER SYS = 0000	-4.0	-1.0	2.0	dB

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Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Sharpness variability range	(trap 1 mid)	Sharp32T1	F = 2.2MHz, FILTER SYS = 000	5.0	8.0	11.0	dB
	(trap 1 max)	Sharp63T1	F = 2.2MHz, FILTER SYS = 000	8.5	11.5	13.5	dB
	(trap 1 min)	Sharp0T1	F = 2.2MHz, FILTER SYS = 000	-6.5	-3.5	-0.5	dB
Sharpness variability range	(trap 2 mid)	Sharp32T1	F = 2.7MHz, FILTER SYS = 010	5.0	8.0	11.0	dB
	(trap 2 max)	Sharp63T1	F = 2.7MHz, FILTER SYS = 010	8.5	11.5	13.5	dB
	(trap 2 min)	Sharp0T1	F = 2.7MHz, FILTER SYS = 010	-6.5	-3.5	-0.5	dB
Sharpness variability range	(trap 3 mid)	Sharp32T1	F = 3.0MHz, FILTER SYS = 100	5.0	8.0	11.0	dB
	(trap 3 max)	Sharp63T1	F = 3.0MHz, FILTER SYS = 100	8.5	11.5	13.5	dB
	(trap 3 min)	Sharp0T1	F = 3.0MHz, FILTER SYS = 100	-6.5	-3.5	-0.5	dB
Black stretch gain max		$BK_{ST}max$	Gain = 10, Start = 01	23.0	28.0	33.0	IRE
Black stretch gain mid		$BK_{ST}mid$	Gain = 01, Start = 01	16.0	21.0	26.0	IRE
Black stretch gain min		$BK_{ST}min$	Gain = 00, Start = 01	9.0	14.0	19.0	IRE
Black stretch start point max (60IRE ΔV)		$BK_{ST}THmax$	Bain = 01, Start = 10	-5.0	0.0	+5.0	IRE
Black stretch start point mid (50IRE ΔV)		$BK_{ST}THmid$	Bain = 01, Start = 01	-5.0	0.0	+5.0	IRE
Black stretch start point min (40IRE ΔV)		$BK_{ST}THmin$	Bain = 01, Start = 00	-5.0	0.0	+5.0	IRE
DC transmission amount 1		ClampG1	DCREST = 00	95.0	100.0	105.0	%
DC transmission amount 2		ClampG2	DCREST = 01	102.0	107.0	112.0	%
DC transmission amount 3		ClampG3	DCREST = 10	107.0	112.0	117.0	%
DC transmission amount 4		ClampG4	DCREST = 11	113.0	118.0	123.0	%
Horizontal/vertical blanking output level		RGB_{BLK}		0.1	0.4	0.7	V
Video frequency characteristics 1 6MHz Trap		BW1	3.4MHz/100kHz, Filter sys = 0100	-6.0	-3.0	0.0	dB
Video frequency characteristics 2 PAL		BW2	1.8MHz/100kHz, Filter sys = 0010	-6.0	-3.0	0.0	dB
Video frequency characteristics 3 NTSC		BW3	1.4MHz/100kHz, Filter sys = 0000	-6.0	-3.0	0.0	dB
White peak limiter effective point 1		$W_{PL}1$	APL = 10% WPL = 01	90.0	95.0	100.0	IRE
White peak limiter effective point 2		$W_{PL}2$	APL = 100% WPL = 01	150.0	160.0	170.0	IRE
Y gamma effective point 1		Y_G1	YGAMMA = 01	89.0	93.0	97.0	%
Y gamma effective point 2		Y_G2	YGAMMA = 10	81.0	85.0	89.0	%
Y gamma effective point 3		Y_G3	YGAMMA = 11	76.0	80.0	84.0	%
Pre-shoot adjust 1		PreShoot1	Pre-shoot adj. = 00	0.92	0.97	1.02	
Pre-shoot adjust 2		PreShoot2	Pre-shoot adj. = 11	1.08	1.13	1.18	
[Chroma block] : PAL/NTSC common							
B-Y/Y amplitude ratio		CLR_{BY}		75	100	150	%
Color control characteristics 1		CLR_{MN}	Color MAX/CEN	1.6	2.0	2.4	times
Color control characteristics 2		CLR_{MM}	Color MAX/MIN	33	40	50	dB
Color control sensitivity		CLR_{SE}		1	2	4	%/bit
Residual higher harmonic level B		E_CAR_B				300	mVp-p
Residual higher harmonic level R		E_CAR_R				300	mVp-p
Residual higher harmonic level G		E_CAR_G				300	mVp-p
[Chroma block] : PAL							
ACC amplitude characteristics 1		ACC_{M1_P}	Input : +6dB/0dB 0dB = 40IRE	0.8	1.0	1.2	times
ACC amplitude characteristics 2		ACC_{M2_P}	Input : -20dB/0dB	0.7	1.0	1.1	times
Demodulation output ratio R-Y/B-Y : PAL		RB_P	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center	0.50	0.56	0.67	times
Demodulation output ratio G-Y/B-Y : PAL		GB_P	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center, R-Y = no-signal	-0.21	-0.19	-0.17	times
Demodulation output ratio G-Y/R-Y : PAL		GR_P	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center, B-Y = no-signal	-0.56	-0.51	-0.46	times
Demodulation angle R-Y/B-Y : PAL		ANG_{RB_P}	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center	85	90	95	deg
Killer operating point		KILL_P	0dB = 40IRE	-39	-33	-26	dB

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
APC pull-in range (+)	PULIN+_P		350			Hz
APC pull-in range (-)	PULIN-_P				-350	Hz
[Chroma block] : NTSC						
ACC amplitude characteristics 1	ACC_{M1_N}	Input : +6dB/0dB 0dB = 40IRE	0.8	1.0	1.2	times
ACC amplitude characteristics 2	ACC_{M2_N}	Input :-20dB/0dB	0.7	1.0	1.1	times
Demodulation output ratio R-Y/B-Y : NTSC	RB_N	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center	0.80	0.90	1.00	times
Demodulation output ratio G-Y/B-Y : NTSC	GB_N	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center	0.24	0.30	0.38	times
Demodulation angle B-Y/R-Y : NTSC	ANG_{BR_N}	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center	99	104	109	deg
Demodulation angle G-Y/B-Y : NTSC	ANG_{GB_N}	R-Y/B-Y_GainBalance_DAC, R-Y/B-Y_Angle_DAC = Center	227	240	250	deg
Demodulation angle switch G-Y/B-Y : NTSC	ANG_{GC_N}	G-Y Angle_DAC = 1	243	253	263	deg
Killer operating point	KILL_N	0dB = 40IRE	-40	-35	-28	dB
APC pull-in range (+)	PULIN+_N		350			Hz
APC pull-in range (-)	PULIN-_N				-350	Hz
Tint center	TINCEN		-10	0	+10	deg
Tint variable range (+)	TINT+		35			deg
Tint variable range (-)	TINT-				-35	deg
[Deflection block]						
Horizontal free-running frequency	fH		530	680	830	Hz
Horizontal pull-in range	fH PULL		±400			Hz
Horizontal output pulse width	Hduty		36.1	37.6	39.1	µs
Horizontal output pulse saturation voltage	V Hsat		0	0.2	0.4	V
Vertical free-running cycle 50	VFR50		312.0	312.5	313.0	H
Vertical free-running cycle 60	VFR60		262.0	262.5	263.0	H
Horizontal output pulse phase	HPHCENpal		9.5	10.5	11.5	µs
Horizontal output pulse phase	HPHCENnt		9.5	10.5	11.5	µs
Horizontal position adjustment range	HPHrange	5bit		±2.2		µs
Horizontal position adjustment maximum variability width	HPHstep				200.0	ns
Horizontal blanking left @0	BLK_{L0}	BLKL : 000	7500	8300	9100	ns
Horizontal blanking left @7	BLK_{L7}	BLKL : 111	10800	11600	12400	ns
Horizontal blanking right @0	BLK_{R0}	BLKR : 000	1800	2600	3400	ns
Horizontal blanking right @7	BLK_{R7}	BLKR : 111	-1100	-300	500	ns
Sand castle pulse crest value H	$SAND_{H}$		5.3	5.6	5.9	V
Sand castle pulse crest value M1	$SAND_{M1}$		3.7	4.0	4.3	V
Sand castle pulse crest value L	$SAND_{L}$		0.1	0.4	0.7	V
Sand castle pulse crest value M2	$SAND_{M2}$		1.7	2.0	2.3	V
Burst gate pulse width	BGP_{WD}		3.5	4.0	4.5	µs
Burst gate pulse phase	BGP_{PH}		4.9	5.4	5.9	µs
Horizontal output stop voltage	Hstop		3.30	3.60	3.90	V
X-ray protection circuit operating voltage	V_{XRAY}		0.59	0.69	0.79	V
[Vertical screen size adjustment]						
Vertical ramp output amplitude PAL@64	Vspal64	VSIZE : 1000000	0.75	0.85	0.95	Vp-p
Vertical ramp output amplitude NTSC@64	Vsnt64	VSIZE : 1000000	0.75	0.85	0.95	Vp-p
Vertical ramp output amplitude PAL@0	Vspal0	VSIZE : 0000000	0.40	0.50	0.60	Vp-p
Vertical ramp output amplitude PAL@127	Vspal127	VSIZE : 1111111	1.05	1.20	1.35	Vp-p
[High-voltage dependent vertical size correction]						
Vertical size correction @0	Vsizecomp	VCOMP : 000	0.83	0.88	0.93	ratio

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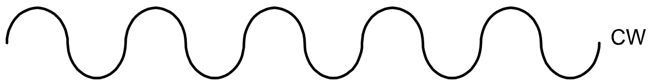
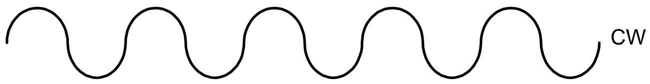
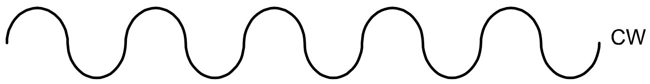
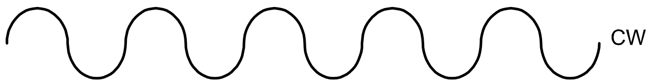
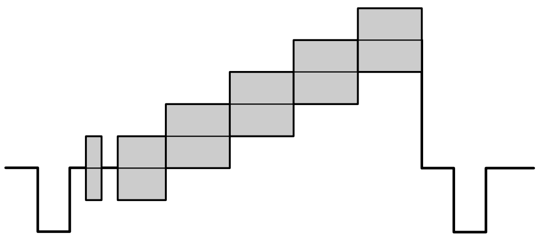
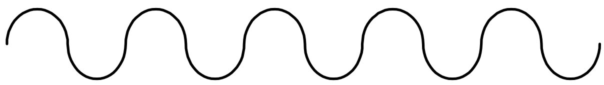
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Vertical screen position adjustment]						
Vertical ramp DC voltage PAL@32	Vdcpal32	VDC : 100000	2.25	2.40	2.55	Vdc
Vertical ramp DC voltage NTSC@32	Vdcnt32	VDC : 100000	2.25	2.40	2.55	Vdc
Vertical ramp DC voltage PAL@0	Vdcpal0	VDC : 000000	1.85	2.00	2.15	Vdc
Vertical ramp DC voltage PAL@63	Vdcpal63	VDC : 111111	2.65	2.80	2.95	Vdc
Vertical linearity @16	Vlin16	VLIN : 10000	0.85	1.00	1.15	ratio
Vertical linearity @0	Vlin0	VLIN : 00000	1.17	1.32	1.47	ratio
Vertical linearity @31	Vlin31	VLIN : 11111	0.57	0.72	0.87	ratio
Vertical S-shaped correction @16	VScor16	VSC : 10000	0.55	0.70	0.85	ratio
Vertical S-shaped correction @0	VScor0	VSC : 00000	0.85	1.00	1.15	ratio
Vertical S-shaped correction @31	VScor31	VSC : 11111	0.36	0.51	0.66	ratio
[Horizontal screen size adjustment]						
East/West DC Voltage@32	EWdc32	EWDC : 100000	1.90	2.30	2.70	Vdc
East/West DC Voltage@0	EWdc0	EWDC : 000000	0.90	1.30	1.70	Vdc
East/West DC Voltage@63	EWdc63	EWDC : 111111	2.90	3.30	3.70	Vdc
[High-voltage dependent horizontal size compensation]						
Horizontal size compensation@0	Hsizecomp	HCOMP : 000	0.1	0.3	0.50	V
[Pincushion correction]						
East/West amplitude@32	EWamp32	EWAMP : 100000	0.90	1.30	1.70	Vp-p
East/West amplitude@0	EWamp0	EWAMP : 000000	-0.40	0.00	+0.40	Vp-p
East/West amplitude@63	EWamp63	EWAMP : 111111	2.20	2.60	3.00	Vp-p
[Correction of trapezoidal distortion]						
East/West parabolic tilt@32	EWtilt32	EWTILT : 100000	-0.40	0.00	+0.40	V
East/West parabolic tilt@0	EWtilt0	EWTILT : 000000	-1.40	-1.00	-0.6	V
East/West parabolic tilt@63	EWtilt63	EWTILT : 111111	0.60	1.00	1.40	V
[Correction of corner distortion]						
East/West parabolic corner top	EWcorTOP	CORTOP : 1111-0000	0.30	0.70	1.10	V
East/West parabolic corner bottom	EWcorBOT	CORBOTTOM : 1111-0000	0.30	0.70	1.10	V

Test Conditions at Ta = 25°C, $V_{CC} = V_8 = V_{31} = V_{43}$ = 5.0V, I_{18} = 19mA, $I_{CC} = I_{25}$ = 27mA

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Circuit voltage, current]					
Horizontal supply voltage (pin 25)	V_{25}	(25)	No signal	Apply a current of 27mA to pin 25 and measure the voltage at pin 25.	Initial
RGB supply voltage (pin 18)	V_{18}	(18)	No signal	Apply a current of 19mA to pin 18 and measure the voltage at pin 18.	Initial
IF supply current (pin 8)	I_8 ($CDDI_{CC}$)	[8]	No signal	Apply a voltage of 5.0V to pin 8 and measure the incoming DC current (mA). (IF AGC 2.5V applied)	Initial
CCD supply current (pin 31)	I_8 ($CDDI_{CC}$)	[31]	No signal	Apply a voltage of 5.0V to pin 31 and measure the incoming DC current (mA).	Initial
Video/vertical supply current (pin 43)	I_{43} ($DEFI_{CC}$)	[43]	No signal	Apply a voltage of 5.0V to pin 43 and measure the incoming DC current (mA).	Initial

VIF Block Input Signals and Test Conditions

1. Input signals must all be input to the PIF IN (pin 6) in the Test Circuit.
2. All input signal voltage values are the levels at the VIF IN (pin 6) in the Test Circuit.
3. Signal contents and signal levels
4. Bus control condition : VIF SYS = ”10”

Input signal	Waveform	Conditions
SG1		45.75MHz
SG2		42.17MHz
SG3		41.25MHz
SG4		Frequency variable
SG5		45.75MHz 87.5% Video Mod. 10-stairstep wave (Subcarrier : 3.58MHz)
SG6		45.75MHz fm = 15kHz, AM = 78%

5. Before measurement, adjust the DAC as follows.

Parameter	Test point	Input signal	Test method
Video Level DAC	46	SG6, 80dBµ	Set the output level at pin 46 as close to 2.0Vp-p as possible.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[VIF block]					
Maximum RF AGC voltage	$V_{RF}H$	4	SG1 80dBμ	Measure the DC voltage at pin 4.	RF. AGC = ”000000”
Minimum RF AGC voltage	$V_{RF}L$	4	SG1 80dBμ	Measure the DC voltage at pin 4.	RF. AGC = ”111111”
RF AGC Delay Pt (@DAC = 0)	$RF_{AGC}0$	4	SG1	Obtain the input level at which the DC voltage at pin 4 becomes 4.5V.	RF. AGC = ”000000”
RF AGC Delay Pt (@DAC = 63)	$RF_{AGC}63$	4	SG1	Obtain the input level at which the DC voltage at pin 4 becomes 4.5V.	RF. AGC = ”111111”
Input sensitivity	V_i	46	SG6	Using an oscilloscope, observe the level at pin 46 and obtain the input level at which the waveform's p-p value becomes 1.4Vp-p.	
No-signal video output voltage	VOn	46	No signal	Set IF AGC = “1” and measure the DC voltage at pin 46.	
Sync signal tip level	VOtip	46	SG1 80dBμ	Measure the DC voltage at pin 46.	
Video output amplitude	VO	46	SG6 80dBμ	Using an oscilloscope, observe the level at pin 46 and measure the waveform’s p-p value.	
Video S/N	S/N	46	SG1 80dBμ	Measure the noise voltage (Vsn) at pin 46 with an RMS voltmeter through a 10kHz to 4.2MHz band-pass filter and calculate 20Log (1.43/Vsn).	
C-S beat level	IC-S	46	SG1 SG2 SG3	Input a 80dBμ SG1 signal and measure the DC voltage (V3) at pin 3. Mix SG1 = 74dBμ, SG2 = 64dBμ, and SG3 = 64dBμ to enter the mixture in the VIF IN. Apply V3 to pin 3 from an external DC power supply. Using a spectrum analyzer, measure the difference between pin 46’s 3.58MHz component and 920MHz component.	
Differential gain	D_G	46	SG5 80dBμ	Using a vector scope, measure the level at Pin 46.	
Differential phase	D_P	46	SG5 80dBμ	Using a vector scope, measure the level at Pin 46.	
Maximun AFT output voltage	$V_{AFT}H$	10	SG4 80dBμ	Set and input the SG4 frequency to 44.75MHz to be input. Measure the DC voltage at pin 10 at that moment.	
Minimun AFT output voltage	$V_{AFT}L$	10	SG4 80dBμz	Set and input the SG4 frequency to 46.75MHz to be input. Measure the DC voltage at pin 10 at that moment.	
AFT detection sensitivity	$V_{AFT}S$	10	SG4 80dBμz	Adjust the SG4 frequency and measure frequency deviation Δf when the DC voltage at pin 10 changes from 1.5V to 3.5V. $V_{AFT}S$ = 2000/Δf [mV/kHz]	
APC pull-in range (U), (L)	f_{PU}, f_{PL}	46	SG4 80dBμ	Connect an oscilloscope to pin 46 and adjust the SG4 frequency to a frequency higher than 45.75MHz to bring the PLL into unlocked mode. (A beat signal appears.) Lower the SG4 frequency and measure the frequency at which the PLL locks again. In the same manner, adjust the SG4 frequency to a lower frequency to bring the PLL into unlocked mode. Lower the SG4 frequency and measure the frequency at which the PLL locks again.	

SIF Block (FM block) Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. Bus control condition : IF. AGC. SW = “1”, SIF.SYS = ”00”, DEEM-TC = ”1”, FM.GAIN = ”1”
2. SW : IF1 = “ON”
3. Input signals are input to pin 54 and the carrier frequency is 4.5MHz.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
FM detection output voltage	SO_{ADJ}	2	90dBμ, fm = 400Hz, FM = ±25kHz	Adjust the DAC (FM. LEVEL) such that the 400 Hz component of the FM detection output at pin 2 become as close to 500 mVrms as possible and measure (SV1 : mVrms) the output at that moment.	
FM limiting sensitivity	S_{LS}	2	fm = 400Hz, FM = ±25kHz	Measure the input level (dBμ) at which the 400Hz component of the FM detection output at pin 2 becomes -3dB relative to SV1.	FM level = Adjustment value
FM detection output f characteristics (fm=100kHz)	S_F	2	90dBμ, fm = 100kHz, FM = ±25kHz	Set SW : IF1 = "OFF". Measure (SV2 : mVrms) the FM detection output of pin 2. Calculate as follows : S_F = 20Log (SV1/SV2) [dB]	FM level = Adjustment value
FM detection output distortion	S_{THD}	2	90dBμ, fm = 400Hz, FM = ±25kHz	Measure the distortion factor of the 400Hz component of the FM detection output at pin 2.	FM level = Adjustment value
AM rejection ratio	S_{AMR}	2	90dBμ, fm = 400Hz, AM = 30%	Measure the 1kHz component (SV3 : mVrms) of the FM detection output at pin 2. Assign the measured value to SV3 and calculate as follows : S_{AMR} = 20Log (SV1/SV3) [dB]	FM level = Adjustment value
SIF. S/N	S_{SN}	2	90dBμ, CW	Measure the noise level (DIN AUDIO, SV4 : mVrms) at pin 2. Calculate as follows : S_{SN} = 20Log (SV1/SV4) [dB]	FM level = Adjustment value
NT de-emph time constant	S_{NTC}	2	90dBμ, fm = 2.12kHz, FM = ±25kHz	Measure the 2.12kHz component (SV5 : mVrms) of the FM detection output at pin 2 and calculate as follows : S_{NTC} = 20Log (SV1/SV5) [dB]	FM level = Adjustment value

Audio Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

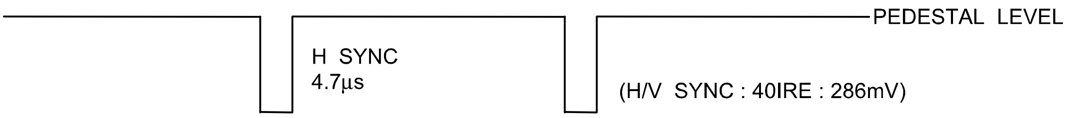
1. Bus control condition : AUDIO. MUTE = ”0”, AUDIO. SW = ”1”, VOL. FIL = ”0” , SIF. SYS = ”00”,
   IF. AGC. SW = ”1”
2. Input 4.5MHz, 90dBμ and CW at pin 54.
3. Enter an input signal from pin 51.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Maximum gain	AG_{MAX}	1	1kHz, CW 500mVrms	Measure the 1kHz component (V1 : mVrms) at the pin 1 and calculate as follows : AG_{MAX} = 20Log (V1/500) [dB]	VOLUME = "1111111"
Variable range	A_{RANGE}	1	1kHz, CW 500mVrms	Measure the 1kHz component (V2 : mVrms) at the pin 1 and calculate as follows : A_{RANGE} = 20Log (V1/V2) [dB]	VOLUME = "0000000"
Frequency characteristics	A_F	1	20kHz, CW 500mVrms	Measure the 20kHz component (V3 : mVrms) at the pin 1 and calculate as follows : A_F = 20Log (V3/V1) [dB]	VOLUME = "1111111"
Mute	A_{MUTE}	1	20kHz, CW 500mVrms	Measure the 20kHz component (V4 : mVrms) at the pin 1 and calculate as follows : A_{MUTE} = 20Log (V3/V4) [dB]	VOLUME = "1111111" AUDIO.MUTE = ”1”
Distortion	A_{THD}	1	1kHz, CW 500mVrms	Measure the distortion of the 1kHz component at the pin 1.	VOLUME = "1111111"
S/N	A_{SN}	1	No signal	Measure the noise level (DIN AUDIO, V5 : mVrms) at the pin 1 and calculate as follows : A_{SN} = 20Log (V1/V5) [dB]	VOLUME = "1111111"
Crosstalk	A_{CT}	1	1kHz, CW 500mVrms	Measure the 1kHz component (V6 : mVrms) at the pin 1 and calculate as follows : A_{CT} = 20Log (V1/V6) [dB]	VOLUME = "1111111" AUDIO. SW = "0"

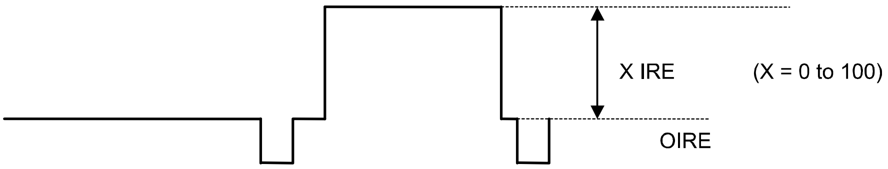
Video Block Input Signals and Test Conditions

1. C IN Input∗chroma burst signal : 40 IRE
2. Y IN input signal 100IRE : 714mV
3. Bus control bit conditions : Initial test state

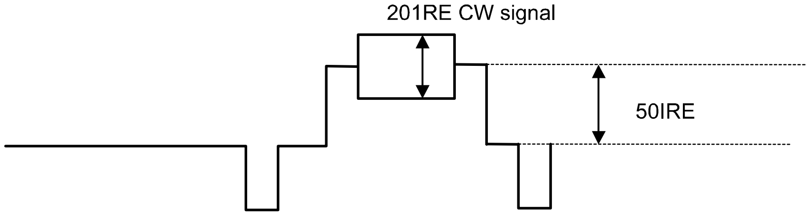
∗OIRE signal (L-O) : NTSC standard sync signal



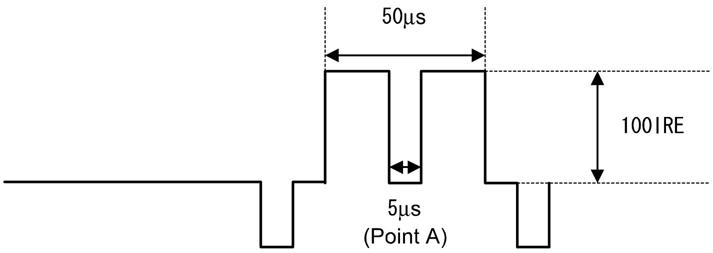
∗XIRE signal (L-X)



∗CW signal (L-CW)

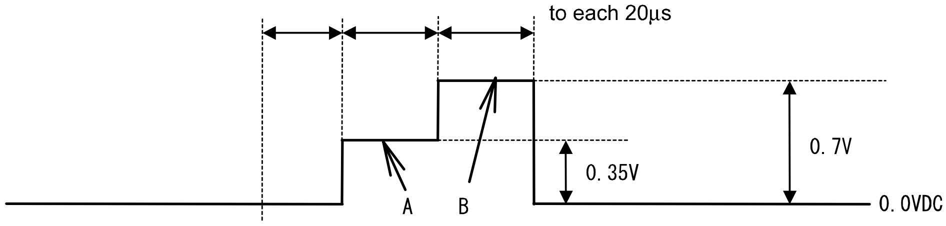


∗BLACK STRETCH OIRE signal (L-BK)

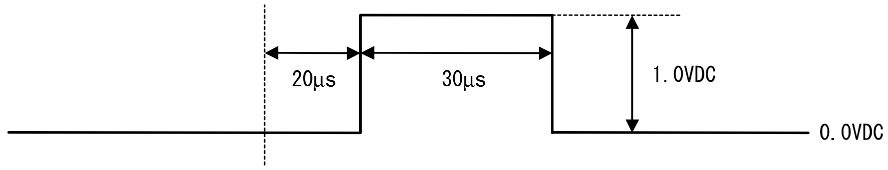


4. R/G/B IN Input signal

RGB Input signal 1 (O-1)



RGB Input signal 2 (O-2)



Parameter	Symbol	Test point	Input signal	Test method	Bus bit/input signal
[Video block]					
Video overall gain (Contrast max)	CONT127	21	L-50	Measure the output signal's 50IRE amplitude (CNTHB Vp-p) and calculate CONT127 = 20Log (CNTHB/0.357).	CONTRAST : 1111111
Contrast adjustment characteristics (normal/max)	CONT63	21	L-50	Measure the output signal's 50IRE amplitude (CNTCB Vp-p) and calculate CONT63 = 20Log (CNTCB/0.357).	CONTRAST : 0111111
Contrast adjustment characteristics (min/max)	CONT0	21	L-50	Measure the output signal's 50IRE amplitude (CNTLB Vp-p) and calculate CONT0 = 20Log (CNTLB/0.357).	CONTRAST : 0000000
Video frequency Characteristics 1 (SVHS)	BW1	21	L-CW	With the input signal's continuous wave = 100kHz, measure the output signal's continuous wave amplitude (PEAKDC Vp-p). With the input signal's continuous wave = 6MHz, measure the output signal's continuous wave amplitude (CW1.4 Vp-p). Calculate BW1 = 20Log (CW1.4/PEAKDC).	FILTER SYS : 000 SHARPNESS : 000000
Video frequency Characteristics 2 (PAL)	BW2	21	L-CW	With the input signal's continuous wave = 1.8MHz, measure the output signal's continuous wave amplitude (CW1.8 Vp-p). Calculate BW2 = 20Log (CW1.8/PEAKDC).	FILTER SYS : 010 SHARPNESS : 000000
Video frequency Characteristics 3 (NTSC)	BW3	21	L-CW	With the input signal's continuous wave = 3.4MHz, measure the output signal's continuous wave amplitude (CW3.4 Vp-p). Calculate BW3 = 20Log (CW3.4/PEAKDC).	FILTER SYS : 100 SHARPNESS : 000000
Chroma trap amount PAL	CtraPP	21	L-CW	With the input signal's continuous wave = 4.43MHz, measure the output signal's continuous wave amplitude (F0P Vp-p). Calculate CtraP = 20Log (F0P/PEAKDC).	FILTER SYS : 010 SHARPNESS : 000000
Chroma trap amount NTSC	CtraPN	21	L-CW	With the input signal's continuous wave = 3.58MHz, measure the output signal's continuous wave amplitude (F0N Vp-p). Calculate CtraN = 20Log (F0N/PEAKDC).	FILTER SYS : 000 SHARPNESS : 000000

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Parameter		Symbol	Test point	Input signal	Test method	Bus bit/input signal
DC transmission amount		ClampG	21	L-0	Measure the output signal's 0IRE DC level (BRTPL V).	Brightness : 0000000 CONTRAST : 1111111
				L-100	Measure the output signal's 0IRE DC level (DRVPH V) and 100IRE amplitude (DRVH Vp-p) and calculate ClampG = 100× (1+ (DRVPH-BRTPL)/DRVH).	Brightness : 0000000 CONTRAST : 1111111
Y-DL TIME1 (SVHS)		T_dY1	21	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	FILTER SYS : 0100
Y-DL TIME2 (PAL)		T_dY2	21	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	FILTER SYS : 0010
Y-DL TIME3 (NTSC)		T_dY3	21	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	FILTER SYS : 0000
Y-DL TIME4 (SECAM)		T_dY4	21	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	FILTER SYS : 1000
Maximum black stretch gain		$BK_{ST}max$	21	L-BK	Measure the 0IRE DC level (BKST1 V) at point A of the output signal in the Black Stretch Defeat (Black Stretch OFF) mode.	
					Measure the 0IRE DC level (BKST2 V) at point A of the output signal in the Black Stretch ON mode.	Blk Str DEF : 0
					Calculate $BK_{ST}max$ = 2×50× (BKST1-BKST2) /CNTHB.	
Black stretch threshold Δblack (60IRE Δblack)		$BK_{ST}TH\Delta$	21	L-60	Measure the 60IRE DC level (BKST3 V) of the output signal in the Black Stretch Defeat ON mode.	Blk Str DEF : 0
					Measure the 60IRE DC level (BKST4 V) of the output signal in the Black Stretch Defeat (Black Stretch OFF) mode.	
					Calculate $BK_{ST}TH\Delta$ = 50× (BKST4-BKST3)/CNTHB.	
Sharpness variability characteristics	(normal)	Sharp31	21	L-CW	With the input signal's continuous wave = 2.2MHz, measure the output signal's continuous wave amplitude (F00S31 Vp-p).	FILTER SYS : 0000 Sharpness : 100000
					Calculate Sharp31 = 20Log (F00S31/PEAKDC).	
	(max)	Sharp63		L-CW	With the input signal's continuous wave = 2.2MHz, measure the output signal's continuous wave amplitude (F00S63 Vp-p).	FILTER SYS : 0000 Sharpness : 111111
					Calculate Sharp63 = 20Log (F00S63/PEAKDC).	
	(min)	Sharp0		L-CW	With the input signal's continuous wave = 2.2MHz, measure the output signal's continuous wave amplitude (F00S0 Vp-p).	FILTER SYS : 0000 Sharpness : 000000
					Calculate Sharp0 = 20Log (F00S0/PEAKDC).	
Horizontal/vertical blanking output level		RGB_{BLK}	21	L-100	Measure the DC level (RGBBLK V) for the output signal's blanking period.	
[OSD block]					Bus control bit conditions : Contrast=63, Brightness=63	Contrast : 0111111 Brightness : 0111111
OSD Fast SW threshold		FSTH	21	L-0 O-2	Apply voltage to pin 17 and measure the voltage at pin 17 at the point where the output signal switches to the OSD signal.	Pin 16A : O-2 applied
Red RGB output level		$R_{OSD}C$	19	L-50	Measure the output signal's 50IRE amplitude (CNT_{CR} Vp-p).	
				L-0 O-2	Measure the OSD output amplitude (OSD_{HR} Vp-p).	Pin 17 : 3.5V Pin 14A : O-2 applied
					Calculate $R_{OSD}H$ = 50× (OSD_{HR}/CNT_{CR}).	

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Parameter		Symbol	Test point	Input signal	Test method	Bus bit/input signal
Green RGB output level		$G_{OSD}C$	20	L-50	Measure the output signal's 50IRE amplitude (CNT_{CG} Vp-p).	
				L-0 O-2	Measure the OSD output amplitude (OSD_{HG} Vp-p).	Pin 17 : 3.5V Pin 15A : O-2 applied
					Calculate $G_{OSD}C = 50\times (OSD_{HG}/CNT_{CG})$.	
Blue RGB output level		$B_{OSD}C$	21	L-50	Measure the output signal's 50IRE amplitude (CNT_{CB} Vp-p).	
				L-0 O-2	Measure the OSD output amplitude (OSD_{HB} Vp-p).	Pin 17 : 3.5V Pin 16A : O-2 applied
					Calculate $B_{OSD}C = 50\times (OSD_{HB}/CNT_{CB})$	
Analog OSD R output level			19	L-0 O-1	Measure the amplitudes at point A (0.35V portion of the input signal 0-1) and point B (0.7V portion of the input signal 0-1) of the output signal. Assign the measured values to RGB_{LR} Vp-p and RGB_{HR} Vp-p, respectively.	Pin 17 : 3.5V Pin 14A : O-1 applied
	Gain match	R_{RGB}			Calculate $R_{RGB} = RGB_{LR}/CNT_{CR}$.	
	linearity	LR_{RGB}			Calculate $LR_{RGB} = 100\times (RGB_{LR}/RGB_{HR})$.	
Analog OSD G output level			20	L-0 O-1	Measure the amplitudes at point A (0.35V portion of the input signal 0-1) and point B (0.7V portion of the input signal 0-1) of the output signal. Assign the measured values to RGB_{LG} Vp-p and RGB_{HG} Vp-p, respectively.	Pin 17 : 3.5V Pin 15A : O-1 applied
	Gain match	G_{RGB}			Calculate $G_{RGB} = RGB_{LG}/CNT_{CG}$.	
	linearity	LG_{RGB}			Calculate $LG_{RGB} = 100\times (RGB_{LG}/RGB_{HG})$.	
Analog OSD B output level			21	L-0 O-1	Measure the amplitudes at point A (0.35V portion of the input signal 0-1) and point B (0.7V portion of the input signal 0-1) of the output signal. Assign the measured values to RGB_{LB} Vp-p and RGB_{HB} Vp-p, respectively.	Pin 17 : 3.5V Pin 16A : O-1 applied
	Gain match	B_{RGB}			Calculate $B_{RGB} = RGB_{LB}/CNT_{CB}$.	
	linearity	LB_{RGB}			Calculate $LB_{RGB} = 100\times (RGB_{LB}/RGB_{HB})$.	
[RGB output block] (Cutoff, drive block)					Bus control bit conditions : Contrast = 127	Contrast : 1111111
Brightness control	(normal)	BRT63	19 20 21	L-0	Measure the 0IRE DC levels of the respective output signals of R output (19), G output (20), and B output (21). Assign the measured values to BRTPCR, BRTPCG, and BRTPCB V, respectively.	Brightness : 01111111
					Calculate BRT63 = (BRTPCR+BRTPCG+BRTPCB) /3.	
	(max)	BRT127	21		Measure the 0IRE DC level of the output signal of B output (21) and assign the measured value to BRTPHB.	Brightness : 1111111
					Calculate BRT127 = 50× (BRTPHB-BRTPCB)/CNTHB.	
	(min)	BRT0			Measure the 0IRE DC level of the output signal of B output (21) and assign the measured value to BRTPLB.	Brightness : 0000000
					Calculate BRT0 = 50× (BRTPLB-BRTPCB)/CNTHB.	

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Parameter		Symbol	Test point	Input signal	Test method	Bus bit/input signal
Bias (cutoff) control	(min)	$V_{bias}0$	19 20 21	L-50	Measure the 0IRE DC levels (Vbias0* V) of the respective output signals of R output (19), G output (20), and B output (21). * : R, G, and B	Sub-Brightness : 0000000
	(max)	$V_{bias}255$			Measure the 0IRE DC levels (Vbias255* V) of the respective output signals of R output (19), G output (20), and B output (21). * : R, G, and B	Sub-Brightness : 1111111 Red/Green/Blue Bias : 11111111
Bias (cutoff) control resolution		$V_{bias}sns$			Measure the 0IRE DC levels (BAS80* V) of the respective output signals of R output (19), G output (20), and B output (21). * : R, G, and B	Red/Green/Blue Bias : 01010000
					Measure the 0IRE DC levels (BAS48* V) of the respective output signals of R output (19), G output (20), and B output (21).	Red/Green/Blue Bias : 00110000
					Calculate Vbiassns* = (BAS80*-BAS48*) /32	
Sub-bias control resolution		$Vs_{bias}sns$		L-50	Measure the 0IRE DC levels (SBTPM* V) of the respective output signals of R output (19), G output (20), and B output (21).	Sub-Brightness : 0101010 Contrast : 0111111
					Calculate Vsbiassns* = (BRTPC*-SBTPM*)	
Drive adjustment maximum output		RBout127 Gout15	19 20 21	L-100	Measure the 100IRE amplitudes (DRVH* Vp-p) of the respective output signals of R output (19) and B output (21). * : R and B Measure the 100IRE amplitude of the output signal of G output (20) and assign the measured value to DRVH* Vp-p. * : G	Brightness : 0000000
Output attenuation		RBout0			Measure the 100IRE amplitudes (DRVL* Vp-p) of the respective output signals of R output (19), G output (20), and B output (21). * : R and B Measure the 100IRE amplitude of the output signal of G output (20) and assign the measured value to DRVL* Vp-p. * : G	Brightness : 0000000 Red/Blue Drive : 0000000
		Gout0			RBout0* = 20Log (DRVH*/DRVL*) Gout0* = 20Log (DRVH*/DRVL*)	
					Bus control bit conditions : Contrast = 63, Brightness = 63	Contrast: 0111111 Brightness : 01111111
[VIDEO SW block]						
Video signal input 1DC voltage		$V_{IN}1_{DC}$	42	L-100	Input signals to pin 42 and measure the voltage of the pedestal.	VIDEO SW : 1
Video signal input 2DC voltage		$V_{IN}2_{DC}$	44	L-100	Input signals to pin 44 and measure the voltage of the pedestal.	VIDEO SW : 0
SVO terminal DC voltage		SVO_{DC}	40	L-100	Input signals to pin 42 and measure the voltage of the pedestal at pin 40.	VIDEO SW : 1
SVO terminal AC voltage		SVO_{AC}	40	L-100	Input signals to pin 42 and measure the voltage of the pedestal at pin 40.	VIDEO SW : 1

Chroma Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. VIF, SIF blocks : No signal

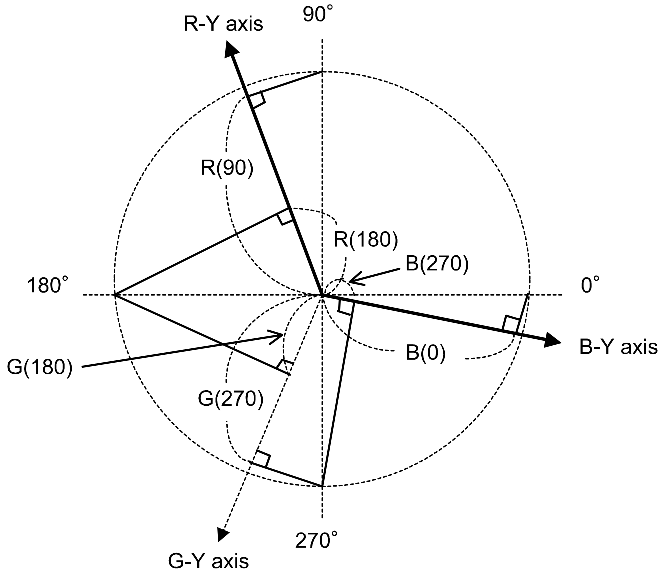
2. Deflection Block : Horizontal/vertical composite sync signals are input and the deflection block must be locked into the sync signals (Refer to the Deflection Block Input Signals and the Test Conditions).

3. Bus control conditions : Set the following conditions unless otherwise specified.
   Y Input is 42 Pin (EXT-V IN),
   C Input is 44 Pin (S-C IN)
   (Video SW = 1, C. Ext = 1)
   Other DAC except the above-mentioned conditions is all initial conditions.

4. Y Input condition: No signal unless otherwise specified.
   (Sync is necessary to obtain synchronization).

5. How to calculate the demodulation ratio and angle :

   B-Y axis angle = tan-1 (B (0) /B (270)) +270°
   R-Y axis angle = tan-1 (R (180) /R (90)) +90°
   G-Y axis angle = tan-1 (G (270) /G (180)) +180°



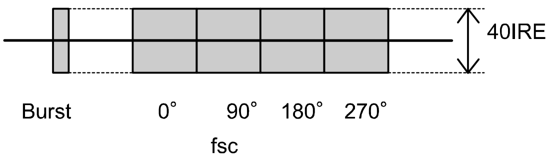
   B-Y axis amplitude Vb = SQRT (B (0) ∗ B (0) +B (270) ∗B (270))
   R-Y axis amplitude Vr = SQRT (R (180) ∗R (180) +R (90) ∗R (90))
   G-Y axis amplitude Vg = SQRT (G (180) ∗G (180) +G (270) ∗G (270))

6. Chroma input signal :

As for the PAL signal, the burst swings such as 130° and 225° every one hour.
Chroma describes the phase caused when the burst occurs at 135°.
As for the NTSC signal, the burst occurs constantly at 180°.
The figures below are based on the phase of NTSC. When a PAL signal is generated, adjust the phase and then enter signals.
The item common to both PAL and NTSC is the PAL signal. For those other than this, the measurement must be performed for each individual signals.
The condition of fsc: Set the following conditions unless otherwise specified.

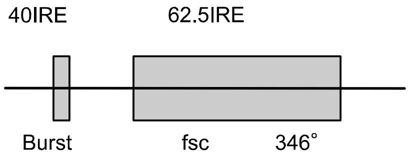
PAL = 4.433619MHz
NTSC = 3.579545MHz

C-1

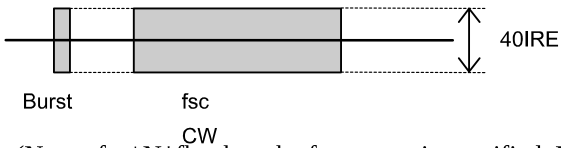


X IRE signal (L-X)

C-2

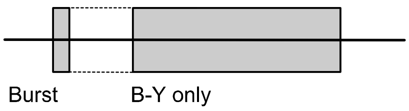


C-3

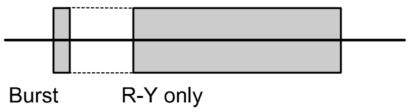


(Note : fsc±N*fh when the frequency is specified. N should be a natural number and the nearest value should be used.)

C-4



C-5



Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Chroma block] : PAL/NTSC common					
B-Y/Y amplitude ratio	CLR_{BY}	Bout 21	YIN : L77 CIN : No signal	Measure the Y system's output level. V1	
			C-2	Input a signal to the CIN (only sync signal to the YIN) and measure the output level to calculate as follows : CLR_{BY} = 100× (V2/V1)+15%	Color : 1000000
Color control characteristics 1	CLR_{MN}	21	C-1	Measure the output amplitude V1 at color control MAX mode and output amplitude V2 at color control CEN mode and, calculate as follows : CLR_{MN} = V1/V2	Color : 1111111 Color : 1000000
Color control characteristics 2	CLR_{MM}	21	C-1	Measure the output amplitude V3 at color control MIN mode to calculate as follows : CLR_{MM} = 20Log (V1/V3)	Color : 0000000
Color control sensitivity	CLR_{SE}	21	C-1	Measure the output amplitude V4 at color control 90 mode and output amplitude V5 at color control 38 mode to calculate as follows : CLR_{SE} = 100× (V4-V5) / (V2×52)	Color : 1011010 Color : 0100110
Residual higher harmonic level B	E_CAR_B	21	C-1 Burst only	Measure the 8.86MHz component output amplitude at pin 21.	
Residual higher harmonic level R	E_CAR_R	Rout 19	Burst only	Measure the 8.86MHz component output amplitude at pin 19.	
Residual higher harmonic level G	E_CAR_G	Gout 20	C-1 Burst only	Measure the 8.86MHz component output amplitude at pin 20.	
[Chroma block] : PAL					
ACC amplitude characteristics 1	ACC_{M1_P}	Bout 21	C-1 0dB +6dB	Measure the output amplitude when 0dB is applied to the chroma input and the output amplitude when +6dB is applied to the chroma input and calculate the ratio between them. ACC_{M1} = 20Log (+6dBdata/0dBdata)	Color : 1000000
ACC amplitude characteristics 2	ACC_{M2_P}	Bout 21	C-1 -20dB	Measure the output amplitude when -20dB is applied to the chroma input and calculate the ratio between them. ACC_{M2} = 20Log (-20dBdata/0dBdata)	Color : 1000000
Demodulation output ratio R-Y/B-Y : PAL	RB_P	21 19	C-1	Refer to 5. and measure Bout output amplitude Vb and R_{OUT} output amplitude Vr. And calculate RB = Vr/Vb.	Color : 1000000
Demodulation output ratio G-Y/B-Y : PAL	GB_P	21 20	C-4	Measure Bout output amplitude Vbp and G_{OUT} output amplitude Vgbp. And calculate GB_P = Vgbp/Vbp.	Color : 1000000
Demodulation output ratio G-Y/R-Y : PAL	GB_P	20 19	C-5	Measure R_{OUT} output amplitude Vrp and G_{OUT} output amplitude Vgbp. And calculate GR_P = Vgrp/Vrp.	Color : 1000000
Demodulation angle R-Y/B-Y : PAL	ANG_{BR_P}	21 19	C-1	Refer to 5. and measure the B-Y and R-Y demodulation angle and calculate.	Color : 1000000
APC pull-in range (+)	PULIN+_P	21	C-1	Decrease the chroma fsc frequency from 4.433619MHz+1000Hz and measure the frequency at which the VCO locks.	
APC pull-in range (-)	PULIN-_P	21	C-1	Increase the chroma fsc frequency from 4.433619MHz-1000Hz and measure the frequency at which the VCO locks.	

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Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Chroma block] : NTSC					
ACC amplitude characteristics 1	ACC_{M1_N}	Bout 21	C-1 0dB +6dB	Measure the output amplitude when 0dB is applied to the chroma input and the output amplitude when +6dB is applied to the chroma input and calculate the ratio between them. ACC_{M1} = 20Log (+6dBdata/0dBdata)	
ACC amplitude characteristics 2	ACC_{M2_N}	Bout 21	C-1 -20dB	Measure the output amplitude when 20dB is applied to the chroma input and calculate the ratio between them. ACC_{M2} = 20Log(-20dBdata/0dBdata)	
Demodulation output ratio R-Y/B-Y : NTSC	RB_N	21 19	C-1	Refer to 5. and measure Bout output amplitude Vb and R_{OUT} output amplitude Vr. And calculate RB = Vr/Vb.	Color : 1000000
Demodulation output ratio R-Y/B-Y : NTSC	GB_N	20	C-1	Refer to 5. and measure G_{OUT} output amplitude Vg. And calculate GB_N = Vg/Vb.	Color : 1000000
Demodulation angle B-Y/R-Y : NTSC	ANG_{BR_N}	21 19	C-1	Refer to 5. and measure the B-Y and R-Y demodulation angle and calculate. Reference : B-Y angle	Color : 1000000
Demodulation angle G-Y/B-Y : NTSC	ANG_{GB_N}	21 20	C-1	Refer to 5. and measure the B-Y and G-Y demodulation angle and calculate. Reference : B-Y angle	Color : 1000000
Killer operating point	KILL_N	21	C-1	Reduce the input signal until the output level becomes 150mVp-p or less. Measure the input level at that moment.	
APC pull-in range (+)	PULIN+_N	21	C-1	Decrease the chroma fsc frequency from 3.579545MHz+1000Hz and measure the frequency at which the VCO locks.	
APC pull-in range (-)	PULIN-_N	21	C-1	Increase the chroma fsc frequency from 3.579545MHz-1000Hz and measure the frequency at which the VCO locks.	
Tint center	TINCEN	21	C-1	Measure each part of the output level and calculate the B-Y axis angle.	TINT : 1000000
Tint variable range (+)	TINT+	21	C-1	Measure each part of the output level and calculate the B-Y axis angle. TINT+ = B-Y axis angle -TINCEN	TINT : 1111111
Tint variable range (-)	TINT-	21	C-1	Measure each part of the output level and calculate the B-Y axis angle. TINT- = B-Y axis angle -TINCEN	TINT : 0000000
[Filter Block Chroma BPF Characteristic]					
C-BPF1A Peaker amplitude characteristic 3.93MHz	CBPF1A	21	C-3 PAL signal	Set the chroma frequency (CW) to 4.433619MHz-100kHz and measure V0 output amplitude. And then, set the chroma frequency (CW) to 3.93MHz and measure V1 output amplitude to calculate as follows : CBPF1A = 20Log (V1/V0)	FILTER SYS = 0010 C. BYPASS = 0
C-BPF1B Peaker amplitude characteristic 4.73/4.13MHz	CBPF1B	21	C-3 PAL signal	Measure V2 output amplitude when the chroma frequency (CW) is 4.13MHz and V3 output amplitude when it (CW) is 4.73MHz to calculate as follows : CBPF1B = 20Log (V3/V2)	FILTER SYS = 0010 C. BYPASS = 0
C-BPF1C Peaker amplitude characteristic 4.93/3.93MHz	CBPF1B	21	C-3 PAL signal	Set the chroma frequency (CW) to 4.93MHz and measure V4 output amplitude to calculate as follows : CBPF1C = 20Log (V4/V1)	FILTER SYS = 0010 C. BYPASS = 0

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Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
C-BPF2A BandPass amplitude characteristic 3.93MHz	CBPF2A	21	C-3 PAL signal	Set the chroma frequency (CW) to 4.433619MHz-100MHz and measure V00 output amplitude. And then, set the chroma frequency (CW) to 3.93MHz and measure V10 output amplitude to calculate as follows : CBPF2A = 20Log (V10/V00)	FILTER SYS = 0011 C. BYPASS = 0
C-BPF2B BandPass amplitude characteristic 4.73/4.13MHz	CBPF2B	21	C-3 PAL signal	Measure V20 output amplitude when the chroma frequency (CW) is 4.13MHz and V30 output amplitude when it (CW) is 4.73MHz to calculate as follows : CBPF2B = 20Log (V30/V20)	FILTER SYS = 0011 C. BYPASS = 0
C-BPF2C BandPass amplitude characteristic 4.93/3.93MHz	CBPF2C	21	C-3 PAL signal	Set the chroma frequency (CW) to 4.93MHz and measure V40 output amplitude to calculate as follows : CBPF2C = 20Log (V40/V10)	FILTER SYS = 0011 C. BYPASS = 0

Deflection Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

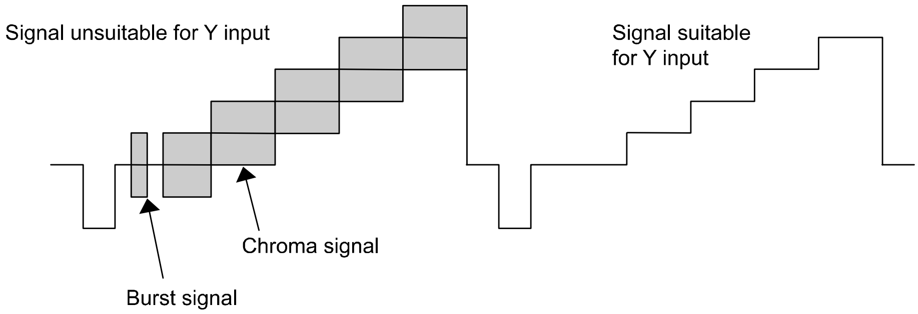
1. VIF, SIF blocks : No signal

2. C input : No signal

3. Sync input : A horizontal/vertical composite sync signal

PAL : 43IRE, horizontal sync signal (15.625kHz) and vertical sync signal (50kHz)
NTSC : 40IRE, horizontal sync signal (15.734264kHz) and vertical sync signal (59.94kHz)

Note : No burst signal, chroma signal shall exist below the pedestal level.



4. Bus control conditions : Initial conditions unless otherwise specified.

5. The delay time from the rise of the horizontal output (pin 27 output) to the fall of the FBP IN (pin 28 input) is 9µs.

6. Pin 13 (vertical size correction circuit input terminal) is connected to V_{CC} (5.0V).

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Deflection block]					
Horizontal free-running frequency	fH	27	Y IN : No signal	Connect a frequency counter to the output of pin 27 (H out) and measure the horizontal free-running frequency.	
Horizontal pull-in range	fH PULL	42	Y IN : Horizontal /vertical sync signal PAL	Using an oscilloscope, monitor the horizontal sync signal which is input to the Y IN (pin 42) and the pin 27 output (H out) and vary the horizontal signal frequency to measure the pull-in range.	
Horizontal output pulse length	Hduty	27	Y IN : Horizontal /vertical sync signal PAL	Measure the voltage for the pin 27 horizontal output pulse's low-level period.	
Horizontal output pulse saturation voltage	V Hsat	27	Y IN : Horizontal /vertical sync signal PAL	Measure the voltage for the pin 27 horizontal output pulse's low-level period.	

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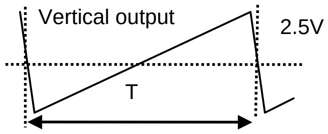
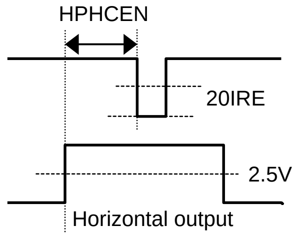
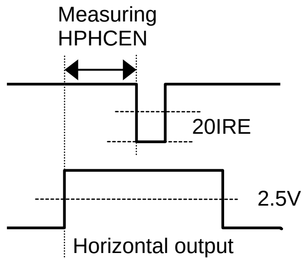
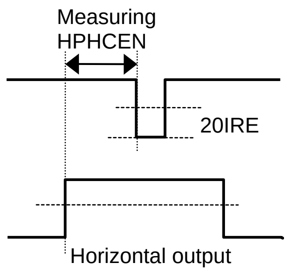
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Vertical free-running period 50 (PAL) Vertical free-running period 60 (NTSC)	VFR50 VFR60	23	Y IN : No signal	Measure the vertical output period T at pin 23. T×15.625kHz (PAL) T×15.734kHz (NTSC) 	CDMODE : 001 (PAL) CDMODE : 002 (NTSC)
Horizontal output pulse (PAL) (NTSC)	HPHCEN (PAL) (NTSC)	27 42	Y IN : Horizontal /vertical sync signal PAL NTSC	Measure the delay time from to the rise of the pin 27 horizontal output pulse to the fall of the Y IN horizontal sync signal. 	
Horizontal position adjustment range	HPHrange	27 42	Y IN : Horizontal /vertical sync signal PAL	With H PHASE : 0 and 31, measure the delay time from the rise of the pin 27 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the difference from H PHCEN. 	H PHASE : 00000 H PHASE : 11111
Horizontal position adjustment maximum variable width	HPHstep	27 42	Y IN : Horizontal /vertical sync signal PAL	With H PHASE : 0 to 31 varied, measure the delay time from to the rise of the pin 27 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the variation at each step. Retrieve data for maximum variation. 	H PHASE : 00000 to H PHASE : 11111
POR circuit operating voltage	VPOR	25	Y IN : Horizontal /vertical sync signal PAL	Connect a DC power supply in place of the current source to pin 25 and gradually decrease the voltage from 5.0V until the BUS READ TATUS [POR] [STATUS1 (DA01) becomes "1". Measure the DC voltage at pin 25 at the moment.	

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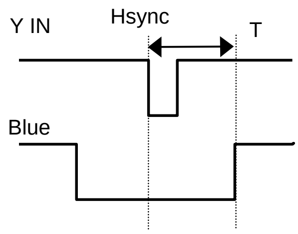
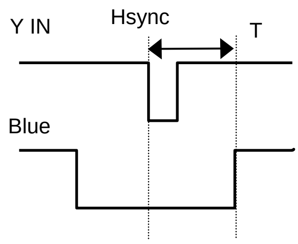
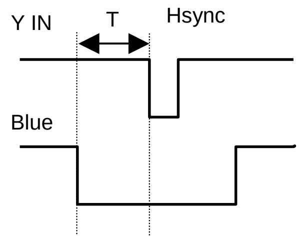
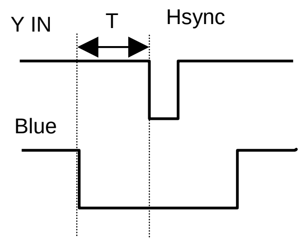
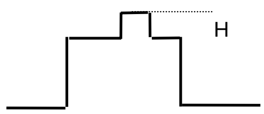
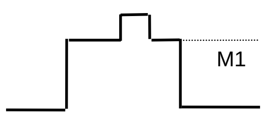
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal blanking left variable range@0	BLK_{L0}	21 42	Y IN : Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKL = 000.  	BLKL : 000
Horizontal blanking left variable range@7	BLK_{L7}	21 42	Y IN : Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKL = 111.  	BLKL : 111
Horizontal blanking right variable range@0	BLK_{R0}	21 42	Y IN : Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKR = 000.  	BLKR : 000
Horizontal blanking right variable range@7	BLK_{R7}	21 42	Y IN : Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKR = 111.  	BLKR : 111
Sand castle pulse crest value H	$SAND_{H}$	28	Y IN : Horizontal /vertical sync signal PAL	Measure the supply voltage at point H of the pin 28 FBP IN wave form for Hsync period.  	
Sand castle pulse crest value M1	$SAND_{M1}$	28	Y IN : Horizontal /vertical sync signal PAL	Measure the supply voltage at point M1 of the pin 28 FBP IN wave form for Hsync period.  	

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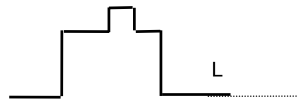
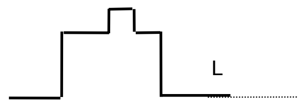
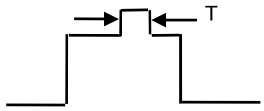
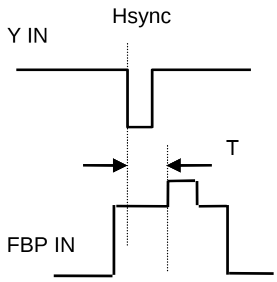
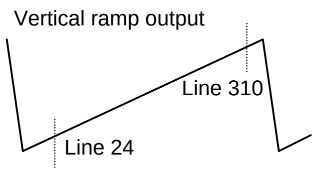
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Sand castle pulse crest value L	$SAND_L$	28	Y IN : Horizontal /vertical sync signal PAL	Measure the supply voltage at point L of the pin 28 FBP IN wave form for Hsync period. 	
Sand castle pulse crest value M2	$SAND_{M2}$	28	Y IN : Horizontal /vertical sync signal PAL	Measure the supply voltage at point M2 of the pin 28 FBP IN wave form for Vsync period. 	
Burst gate pulse length	BGP_{WD}	28	Y IN : Horizontal /vertical sync signal PAL	Measure the BGP width T of the pin 28 FBP IN wave form for Hsync period. 	
Burst gate pulse I phase	BGP_{PH}	28 42	Y IN : Horizontal /vertical sync signal PAL	Measure the time from the left end of Hsync at pin 42 Y IN to the left end of the pin 28 FBP IN wave form for Hsync period. 	
Horizontal output stop voltage	Hstop	25 27	Y IN : Horizontal /vertical sync signal	Decrease the current from a source connected to pin 25 and measure the pin 25 voltage at which HOUT stops.	
X-ray protection circuit operating voltage	V_{XRAY}	27 34	Y IN : Horizontal /vertical sync signal	Connect a DC power supply to pin 34 and gradually increase the voltage from 0V until the pin 27 horizontal output pulse ceases. Measure the DC voltage at pin 34 at that moment.	
[Vertical screen size correction]					
Vertical ramp output amplitude PAL@64 NTSC@64	Vspal64 Vsnt64	23	Y IN : Horizontal /vertical sync signal PAL NTSC	Monitor the pin 23 vertical ramp output and measure the voltage at line 24 and line 310. Calculate as follows : Vspal64 = Vline310-Vline24 Vsnt64 = Vline262-Vline22 	

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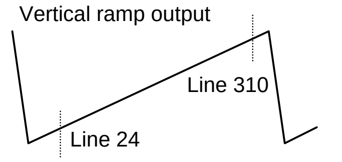
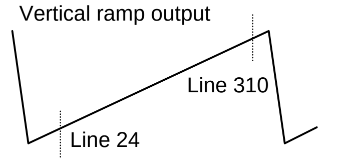
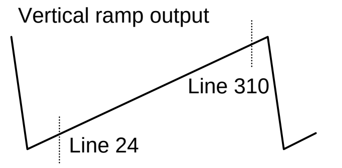
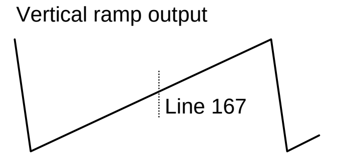
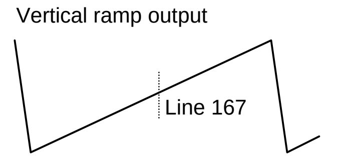
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Vertical ramp output amplitude PAL@0	Vspal0	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 24 and line 310. Calculate as follows : Vspal0 = Vline310-Vline24 	VSIZE : 0000000
Vertical ramp output amplitude PAL@127	Vspal127	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 24 and line 310. Calculate as follows : Vspal27 = Vline310-Vline24 	VSIZE : 1111111
[High-voltage dependent vertical size correction]					
Vertical size correction@0	Vsizecomp	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at the line 24 and line 310 with VCOMP = 000. Calculate as follows : Va = Vline310-Vline24 Apply 4.1V to pin 13 and measure the voltage at the line 24 and line 310 again. Calculate as follows : Va = Vline310-Vline24 Calculate as follows : Vsizecomp = Vb/Va 	VCOMP : 000
[Vertical screen position adjustment]					
Vertical ramp DC voltage PAL@32 NTSC@32	Vdcpal32 Vdcnt32	23	Y IN : Horizontal /vertical sync signal PAL NTSC	Monitor the pin 23 vertical ramp output and measure the voltage at line 167. (PAL) Monitor the pin 23 vertical ramp output and measure the voltage at line 142. (NTSC) 	
Vertical ramp DC voltage PAL@0	Vdcpal0	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 167. 	VDC : 000000

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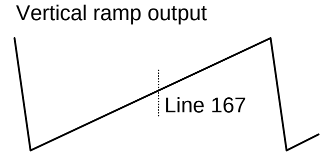
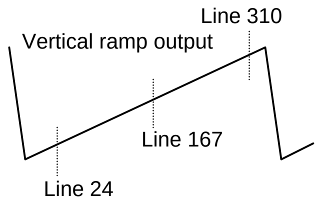
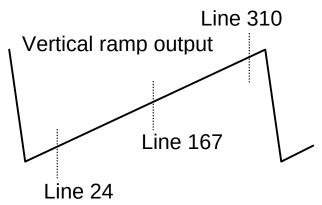
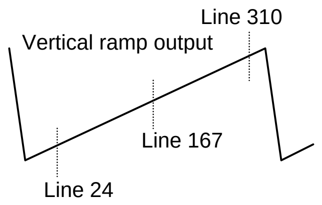
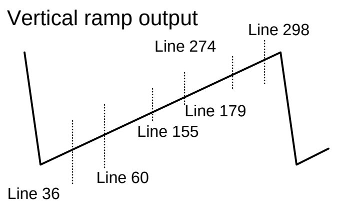
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Vertical ramp DC voltage PAL@63	Vdcpal63	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 167.  	VDC : 111111
Vertical linearity@16	Vlin16	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows : Vlin16 = (Vb-Va) / (Vc-Vb)  	
Vertical linearity@0	Vlin0	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows : Vlin0 = (Vb-Va) / (Vc-Vb)  	VLIN : 00000
Vertical linearity@31	Vlin31	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows : Vlin31 = (Vb-Va) / (Vc-Vb)  	VLIN : 11111
Vertical S-shaped correction @16	VScor16	15	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at line 36, line 60, line 155, line 179, line 274 and 298. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows : VScor16 = 0.5 ((Vb-Va) + (Vf-Ve)) / (Vd-Vc)  	VS : 10000

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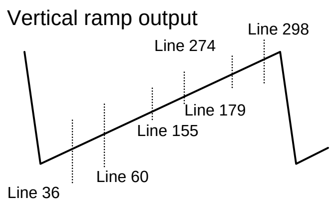
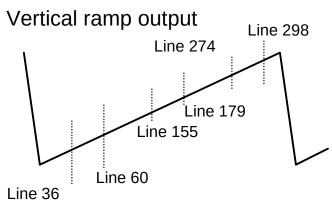
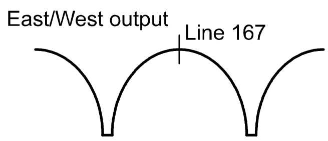
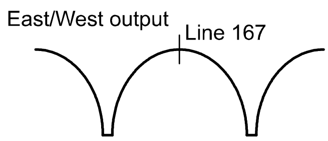
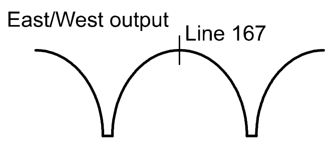
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Vertical S-shaped correction @0	VScor0	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at the line 36, line 60, line 155, line 179, line 274 and line 298 with VSC = 00000. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows : VScor0 = 0.5 ((Vb-Va) + (Vf-Ve)) / (Vd-Vc) 	
Vertical S-shaped correction @31	VScor31	23	Y IN : Horizontal /vertical sync signal PAL	Monitor the pin 23 vertical ramp output and measure the voltage at the line 36, line 60, line 155, line 179, line 274 and line 298 with VSC = 11111. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows : VScor31 = 0.5 ((Vb-Va) + (Vf-Ve)) / (Vd-Vc) 	VSC : 11111
[Horizontal size adjustment]					
East/Wst DC voltage@32	EWdc32	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 167. 	
East/West DC voltage @0	EWdc0	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 167. 	EWDC : 000000
East/West DC voltage @63	EWdc63	22	Y IN : No signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 167. 	EWDC : 111111

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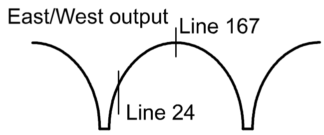
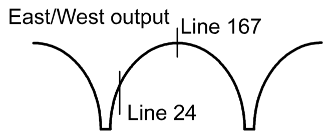
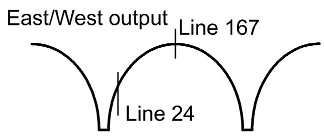
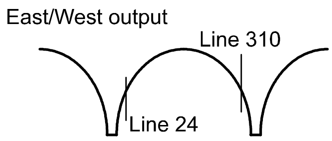
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[High-voltage dependent horizontal size compensation]					
Horizontal size compensation @0	Hsizecomp	22	Y IN : Horizontal /vertical sync signal	Monitor the West/East output of pin 22 and measure the voltage (Va) at line 167. Apply 4.0V to pin 13 and measure again the voltage (Vb) at line 167. Calculate as follows : Hsizecomp = Va-Vb	HCOMP : 000
[Pincushion distortion compensation]					
East/West parabolic amplitude @32	EWamp32	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 24 (Va) and line 167 (Vb). Calculate as follows : EWamp32 = Vb-Va 	
East/West parabolic amplitude @0	EWamp0	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 24 (Va) and line 167 (Vb). Calculate as follows : EWamp32 = Vb-Va 	EWAMP : 000000
East/West parabolic amplitude @63	EWamp63	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 24 (Va) and line 167 (Vb). Calculate as follows : EWamp63 = Vb-Va 	EWAMP : 111111
[Trapezoidal distortion compensation]					
East/West parabolic tilt @32	EWtilt32	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 24 (Va) and line 310 (Vb). Calculate as follows : EWtilt32 = Va-Vb 	

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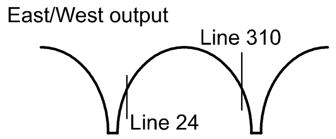
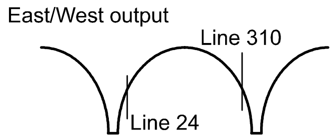
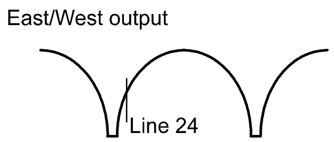
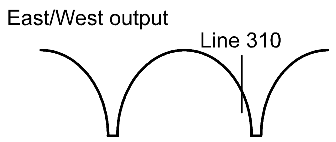
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
East/West parabolic tilt @0	EWtilt0	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 24 (Va) and line 310 (Vb). Calculate as follows : EWtilt32 = Va-Vb 	EWTILT : 000000
East/West parabolic tilt @63	EWtilt63	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 24 (Va) and line 310 (Vb). Calculate as follows : EWtilt32 = Va-Vb 	EWTILT : 111111
[Corner distortion compensation]					
East/West parabolic corner TOP	EWcortop	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 24 under conditions of CORTOP : 1111 (Va) and CORTOP : 0000 (Vb). Calculate as follows : Ewcortop = Va-Vb 	CORTOP : 1111-0000
East/West parabolic corner BOTTOM	EWcorbot	22	Y IN : Horizontal /vertical sync signal	Monitor the East/West output (parabolic wave output) of pin 22 and measure the voltage at line 310 under conditions of CORBOT : 1111 (Va) and CORBOT : 0000 (Vb). Calculate as follows : Ewcorbot = Va-Vb 	CORBOTTOM : 1111-0000

LA76832N Pin Assignment

PIN	FUNCTION	PIN	FUNCTION
1	Audio Output	54	SIF Input
2	FM Output	53	SIF APC Filter
3	PIF AGC	52	SIF Output
4	RF AGC Output	51	Ext. Audio Input
5	PIF Input1	50	APC Filter
6	PIF Input2	49	VCO Coil 1
7	IF Ground	48	VCO Coil 2
8	IF V_{CC}	47	VCO Filter
9	FM Filter	46	Video Output
10	AFT Output	45	Black Level Detector
11	Bus Data	44	Internal Video Input (S-C IN)
12	Bus Clock	43	Video/Vertical V_{CC}
13	ABL	42	External Video Input (Y IN)
14	Red Input	41	Video/Vertical/BUS Ground
15	Green Input	40	Selected Video Output
16	Blue Input	39	Chroma APC1 Filter
17	Fast Blanking Input	38	4.43MHz Crystal
18	RGB V_{CC}	37	Clamp Filter
19	Red Output	36	Chroma APC2 Filter
20	Green Output	35	Fsc or Csync Output
21	Blue Output	34	XRAY
22	E/W Output	33	CCD/Horizontal Ground
23	Vertical Output	32	CCD Filter
24	Ramp ALC Filter	31	CCD V_{CC}
25	Horizontal/BUS V_{CC}	30	Clock (4MHz) Output
26	Horizontal AFC Filter	29	VCO IREF
27	Horizontal Output	28	Flyback Pulse Input

LA76832N BUS Control Register Bit Allocation Map IC Address (WRITE) : 10111010

Sub Address	MSB			DATA BITS			LSB
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7
00000000	ON/OFF	AFC gain & gate	H.FREQ					
	1	0	1	1	1	1	1	1
00001	Vreset Timing	Audio. Mute	Video. Mute	H. PAHSE				
	0	0	0	1	0	0	0	0
00010	Sync. Kill	V. SIZE						
	0	1	0	0	0	0	0	0
00011	VSEPUP	V. KILL	V. POSI					
	0	0	1	0	0	0	0	0
00100	H BLK L			V. LIN				
	1	0	0	1	0	0	0	0
00101	H BLK R			V. SC				
	1	0	0	0	1	0	1	1
00110	V. TEST		V. COMP			COUNT. DOWN. MODE		
	0	0	1	1	1	0	0	0
00111	R. BIAS							
	0	0	0	0	0	0	0	0
01000	G. BIAS							
	0	0	0	0	0	0	0	0
01001	B. BIAS							
	0	0	0	0	0	0	0	0
01010	*	R. DRIVE						
	(0)	1	1	1	1	1	1	1
01011	Drive. Test	Half tone		Half tone Def	G. DRIVE			
	0	0	1	1	1	0	0	0
01100	*	B. DRIVE						
	(0)	1	1	1	1	1	1	1
01101	Blank. Def	Sub. Bias						
	0	1	0	0	0	0	0	0
01110	IF Test1	Bright						
	0	1	0	0	0	0	0	0
01111	IF Test2	Contrast						
	0	1	0	0	0	0	0	0

(Bits are transmitted in this order.)

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Sub Address	MSB				DATA BITS			LSB
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7
00010000	OSD Cnt. Test	OSD Contrast						
	0	1	0	0	0	0	0	0
10001	Blk. Str. Def	Coring	Sharpness					
	1	1	0	0	0	0	0	0
10010	Tint. Test	Tint						
	0	1	0	0	0	0	0	0
10011	Color. Test	Color						
	0	1	0	0	0	0	0	0
10100	Video SW	Trap Test			Filter. Sys			
	0	1	0	0	0	0	1	0
10101	Gray Mode	Cross B/W		*	G-Y Angle	Color killer ope.		
	0	0	0	(0)	(0)	0	0	0
10110	VBLK SW	FBPBLK.	Fsc or Csync	WPL	Pre-shoot adj.		Coring Gain	
	0	1	0	0	0	0	0	0
10111	Y Gamma Start		DC. Rest		Blk. Str. start		Blk. Str. Gain	
	0	0	0	0	0	0	0	0
11000	Auto. Flesh	C. Ext	C. Bypass	C_Kill ON	C_Kill OFF	Color. Sys		
	0	0	1	0	0	0	0	0
11001	Cont. Test	Digital OSD	Brt. Abl. Def	Mid. Stp. Def	RGB Temp	Bright. Abl. Threshold		
	0	0	0	0	0	1	0	0
11010	R-Y/B-Y Gain Balance				R-Y/B-Y Angle			
	1	0	0	0	1	0	0	0
11011	B-Y DC Level (White-Balance)				R-Y DC Level(White-Balance)			
	1	0	0	0	1	0	0	0
11100	Audio SW	Volume						
	0	0	0	0	0	0	0	0
11101	IF Test	VOL. FIL	RF. AGC					
	0	0	1	0	0	0	0	0
11110	FM. Mute	deem. TC	VIF. Sys. SW		SIF. Sys. SW		FM. Gain	IF. AGC
	0	1	1	0	0	0	1	0
11111	VIDEO. LEVEL			FM. LEVEL				
	1	0	0	1	0	0	0	0

(Bits are transmitted in this order.)

LA76832N BUS:Control Register Truth Table

Register Name	0 HEX	1 HEX	2 HEX	3 HEX
ON/OFF (T. Disable)	OFF (Tset Enable)	ON (Test Disable)		
AFC gain & gate	Auto (Gain)	Gain : Fast		
	Auto (Gate)	Non-Gate		
V Reset Timing	Normal	1/4H Shift		
Audio. Mute	Active	Mute		
Video. Mute	Active	Mute		
Sync. Kill	Sync active	Sync killed		
Vsepup	normal	Vsepup		
V. KILL	Vrt active	Vrt killed		
Gray Mode	Normal	Gray OSD		
Cross B/W	Normal	Black	White	Cross
Vertical Test	Normal	Vrt S Corr	Vrt Lin	Vrt Size
Half Tone Def	Half Tone on	Half Tone off		
Drive. Test	Normal	Test Mode		
Blank. Def	Blanking	No Blank		
OSD Cnt. Test	Normal	Test Mode		
Blk. Str. Def	Blk Str On	Blk Str Off		
Coring	Core Off	Core On		
Tint. Test	Normal	Test Mode		
Color. Test	Normal	Test Mode		
Video. SW	Internal Mode	External Mode		
G-Y Angle	240deg	253deg		
VBLK SW	24H to 262H (NTSC)	29H to 256H (NTSC)		
	25H to 309H (PAL)	30H to 304H (PAL)		
Fsc or Csync	35pin : Fsc out	35pin : Csync out		
FBPBLK. SW	FBP not or	FBP or		
WPL	WPL OFF	WPL ON		
Pre-shoot adj.	Normal	+10ns	+20ns	+30ns
Coring Gain	Min	->	->	Max
Y Gamma Start	Y Gamma off	Min	->	Max
DC Rest.	100%	106%	113%	128%
Blk. Str. start	Low	->	High	
Blk. Str. Gain	Min	->	Max	
Auto Flesh	OFF	ON		
C. Ext	Internal Mode	External Mode		
C. Bypass	Bypass OFF	Bypass ON		
C_Kill ON	Auto Mode	Killer ON		
C_Kill OFF	Auto Mode	Killer OFF		
Cont. Test	Normal	Test Mode		
Digital OSD	Analogue	Digital		
Brt. ABL. Def	Brt ABL On	Brt ABL Off		
Mid. Stp. Def	Mid Stp On	Mid Stp Off		
Audio. SW	Internal Mode	External Mode		
VOL. FIL	Normal	Filte OFF		
FM. Mute	Active	Mute		
de-em TC.	50µs	75µs		
VIF. Sys. SW	38.0MHz	38.9MHz	45.75MHz	39.5MHz
SIF. Sys. SW	4.5MHz	5.5MHz	6.0MHz	6.5MHz
FM Gain	50kHz dev.	25kHz dev		
IF. AGC	AGC active	AGC defeat		

LA76832N BUS : Control Register Truth Table

COUNT DOWN MODE

	50Hz/60Hz MODE	Standard/Non-Standard MODE
0 HEX	Auto	Auto
1 HEX	50Hz	Auto
2 HEX	60Hz	Auto
3 HEX	Auto	Auto
4 HEX	Auto	Non-Standard
5 HEX	50Hz	Non-Standard
6 HEX	60Hz	Non-Standard
7 HEX	Auto	Non-Standard

Color System

0 HEX	Auto Mode1 PAL/NTSC/4.43NTSC (/SECAM)
1 HEX	Auto Mode2 PAL-M/PAL-N/NTSC
2 HEX	PAL
3 HEX	PAL-M
4 HEX	PAL-N
5 HEX	NTSC
6 HEX	4.43NTSC
7 HEX	SECAM

Filter System

	Y Filter	Chroma Filter
0 HEX	3.58MHz Trap	Peaked 3.58MHz BPF
1 HEX	3.58MHz Trap	Symmetrical 3.58MHz BPF
2 HEX	4.43MHz Trap	Peaked 4.43MHz BPF
3 HEX	4.43MHz Trap	Symmetrical 4.43MHz BPF
4 HEX	6.0MHz Trap	Peaked 3.58MHz BPF
5 HEX	6.0MHz Trap	Symmetrical 3.58MHz BPF
6 HEX	6.0MHz Trap	Peaked 4.43MHz BPF
7 HEX	6.0MHz Trap	Symmetrical 4.43MHz BPF
8-15HEX	4.286MHz Trap	Symmetrical 4.43MHz BPF

LA76832N BUS : Status Byte Truth Table

Register	0 HEX	1 HEX
XRAY	Undetected	Detected
(POR)	(Undetected)	(Detected)
IF. IDENT	Sync Undetected	Sync Detected
RF. AGC	RF. AGC. OUT = ″L″	RF. AGC. OUT = ″H″
IF. LOCK	Lock	Unlock
V. TRI	V. Triger Undetected	V. Triger Detected
50/60	50	60
ST/NONST	Non-Standard	Standard
H. LOCK	Horiz Unlocked	Horiz Locked
KILLER	KILLER OFF	KILLER ON

Color System	0 HEX	B/W
	1 HEX	PAL
	2 HEX	PAL-M
	3 HEX	PAL-N
	4 HEX	NTSC
	5 HEX	4.43NTSC
	6 HEX	SECAM
	7 HEX	Do not care

LA76832N BUS Initial Conditions

Register	
ON/OFF (T. Disable)	1 HEX
AFC gain & gate	0 HEX
H. FREQ	3F HEX
V Reset Timing	0 HEX
Audio. Mute	0 HEX
Video. Mute	0 HEX
H. PHASE	10 HEX
Sync. Kill	0 HEX
V. SIZE	40 HEX
VSEPUP	0 HEX
V. KILL	0 HEX
V. POSI	20 HEX
V. LIN	10 HEX
V. SC	0B HEX
H BLK L	4 HEX
H BLK R	4 HEX
V. TEST	0 HEX
V. COMP	7 HEX
COUNT. DOWN. MODE	0 HEX
R. BIAS	00 HEX
G. BIAS	00 HEX
B. BIAS	00 HEX
R. DRIVE	7F HEX
Drive Test	0 HEX
Half Tone	1 HEX
Half Tone Def	1 HEX
G. DRIVE	8 HEX
B. DRIVE	7F HEX
Blank. Def	0 HEX
Sub. Bias	40 HEX
Bright	40 HEX
Contrast	40 HEX

East/West DC	20 HEX
East/West Amp	20 HEX
East/West Tilt	20 HEX
East/West Corner TOP	0 HEX
East/West Corner Bottom	0 HEX
East/West Test	0 HEX
H. Size. Comp	7 HEX

RGB Temp SW	0 HEX
IF Test	0 HEX
IF Test1	0 HEX
IF Test2	0 HEX
IF Test3	48 HEX

Register	
OSD Cnt. Test	0 HEX
OSD Contrast	0 HEX
Blk. Str. Def	1 HEX
Coring	1 HEX
Sharpness	00 HEX
Tint. Test	0 HEX
Tint	40 HEX
Color. Test	0 HEX
Color	40 HEX
Video. SW	0 HEX
Trap. Test	4 HEX
Filter. Sys	2 HEX
Gray Mode	0 HEX
Cross B/W	0 HEX
G-Y Angle	0 HEX
Color Killer Ope.	4 HEX
VBLK SW	0 HEX
FBPBLK. SW	1 HEX
Fsc or Csync	0 HEX
WPL	1 HEX
Pre-shoot Adj.	0 HEX
Coring Gain	3 HEX
Y Gamma	0 HEX
DC. Rest.	2 HEX
Blk. Str. start	1 HEX
Blk. Str. Gain	1 HEX
Auto Flesh	0 HEX
C. Ext	0 HEX
C. Bypass	1 HEX
C_Kill ON	0 HEX
C_Kill OFF	0 HEX
Color System	0 HEX
Cont. Test	0 HEX
Digitsl OSD	0 HEX
Brt. Abl. Def	0 HEX
Mid. Stp. Def	0 HEX
Bright. Abl. Threshold	4 HEX
R-Y/B-Y Gain Balance	8 HEX
R-Y/B-Y Angle	8 HEX
B-Y DC Level	8 HEX
R-Y DC Level	8 HEX
Audio. SW	0 HEX
Volume	00 HEX
VOL. FIL	0 HEX
RF. AGC	20 HEX
FM. Mute	0HEX
deem. TC	1HEX
VIF. Sys. SW	2 HEX
SIF. Sys. SW	0 HEX
FM. Gain	1 HEX
IF. AGC	0 HEX
VIDEO. LEVEL	4 HEX
FM. LEVEL	10 HEX

LA76832N Bus Control Register Descriptions

Register Name	Bits	General Description
ON/OFF (T Disable)	1	Enable the horizontal output & Disable the Test SW & enable Audio / Video
AFC Gain & gate	1	Select horizontal first loop gain & H-sync gating on/off
H Freq.	6	Align ES Sample horizontal frequency
V Reset Timing	1	Select Vertical Reset Timing
Audio Mute	1	Disable audio outputs
Video Mute	1	Disable video outputs
H PHASE	5	Align sync to flyback phase
Sync Kill	1	Force free-run mode
Vertical Size	7	Align vertical amplitude
Vsep. up	1	Select vertical sync. separation sensitivity
Vertical Kill	1	Disable vertical output
V POSI (Vertical DC)	6	Align vertical DC bias
H BLK L	3	H-Blanking Control (Left side of the screen)
H BLK R	3	H-Blanking Control (Right side of the screen)
V LIN (Vertical Linearity)	5	Align vertical linearity
Vertical S-Correction	5	Align vertical S-correction
Vertical Test	2	Select vertical DAC test modes
Vertical Size Compensation	3	Align vertical size compensation
Count Down Mode	1	Select vertical countdown mode
Red Bias	8	Align Red OUT DC level
Green Bias	8	Align Green OUT DC level
Blue Bias	8	Align Blue OUT DC level
Red Drive	7	Align Red OUT AC level
Drive Test	1	Enable Drive control DAC test modes
Half Tone	2	Adjust half tone level
Half Tone Defeat	1	Half tone defeat SW
Green Drive	4	Align Green OUT AC level
Blue Drive	7	Align Blue OUT AC level
Blank Def	1	Disable RGB output blanking
Sub Bias	7	Align common RGB DC level
Brightness Control	7	Customer brightness control
Contrast Control	7	Customer contrast control
OSD Contrast Test	1	Enable OSD Contrast DAC test mode
OSD Contrast Control	2	Align OSD AC level
Blk Str Def	1	Disable Black stretch
Coring Enable	1	Enable luminance coring
Sharpness Control	6	Customer sharpness control
Tint Test	1	Enable tint DAC test mode
Tint Control	7	Customer tint control
Color Test	1	Enable color DAC test mode
Color Control	7	Customer color control
Video SW	1	Select Video source
Trap. Test	3	Trap Test
Filter System	3	Select Y/C Filter mode
Gray Mode	1	OSD Gray Tone Enable
Cross B/W	2	Service Test Mode (normal/Black/White/Cross)
G-Y Angle Select	1	Select G-Y Angle
Color Killer Operational Point Select	3	Select Color Killer Operational Point
Vertical Blanking SW	1	Select VBLK Period
FBPBLK. SW	1	Enable RGB Blanking or FBP
Fsc or Csync Output	1	Select 35pin Output (0 : Fsc 1 : Csync)
White Peak Limitter SW	1	Enable WPL
Pre-shoot Adjustmant	2	Select Pre-shoot Width
Coring Gain Select	2	Select Coring Gain

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Register Name	Bits	General Description
Y Gamma Start	2	Select Y Gamma Start Point
DC Restoration Select	2	Select Luma DC Restoration
Blk. Str. Start Point Select	2	Select Black stretch Start Point
Blk. Str. Gain Select	2	Select Black stretch Gain
AutoFlesh	1	Enable AutoFlesh function
C Ext	1	Selected-C In SW on
C Bypass	1	Select Chroma BPF bypass
C Kill On	1	C Kill Mode (1 : Enable Killer circuit)
C Kill Off	1	Disable Killer circuit
Color System	3	Select Color System
Cont Test	1	Enable contrast DAC test mode
Bright ABL Defeat	1	Disable brightness ABL
Bright Mid Stop Defeat	1	Disable brightness mid stop
Bright ABL Threshold	3	Align brightness ABL threshold
Digital OSD SW	1	Select Digital/Analogue OSD
R-Y/B-Y Balance	4	R-Y/B-Y Gain Balance
R-Y/B-Y Angle	4	R-Y/B-Y Angle
B-Y DC Level	4	B-Y DC Level (White-Balance)
R-Y DC Level	4	R-Y DC Level (White-Balance)
Audio SW	1	Select Audio source
Volume Control	7	Customer volume control
Volume Filter Defeat	1	Disable volume DAC filter
RF AGC Delay	6	Align RF AGC threshold
FM Mute	1	Disable FM outputs
de-em TC.	1	Select de-emphasis Time Constant
VIF System SW	2	Select 38.0/38.9/39.5/45.75
SIF System SW	2	Select 4.5/5.5/6.0/6.5
FM Gain	1	Select FM Output Level
IF AGC Defeat	1	Disable IF and RF AGC
Video Level	3	Align IF video level
FM Level	5	Align WBA output level
East/West DC	6	Align East/West DC
East/West Amp	6	Align East/West amplitude
East/West Tilt	6	Align East/West tilt
East/West Corner TOP	4	Align bottom corner correction
East/West Corner Bottom	4	Align top corner correction
East/West Test	3	Select East/West DAC test modes
H. Size. Comp	3	Align horizontal size compensation

RGB TEST	1	Select test modes
IF TEST	1	Select test modes
IF TEST1	1	Select test modes
IF TEST2	1	Select test modes
IF TEST3	8	Select test modes

Description of Read Status

X-RAY	X-ray detection circuit is activated with thyristor by means of the threshold voltage from Gnd to 1Vbe. Simultaneously with activation of thyristor, the H drive pulse is stopped and the thyristor output is sent to BUS. BUS Read enables reading of the real-time state of thyristor. To cancel thyristor operation, it is necessary to lower V_{CC} once. 1HEX : Detected
POR	The POR detection circuit cannot be used in LA76832 and should be ignored. The circuit is operating and performs detection with HV_{CC} = <3.6V. At the same time, the memory for Bus Read is set. (Memory is set at power ON.) To reset the memory, it is necessary to set the ON/OFF control bit to zero once. Since the BUS Read Status and ACK are not returned simultaneously with detection, BUS cannot be read at detection. Failure of ACK return may be useful at detection. For example, the BUS communication start may be timed with ACK at power ON.
RF. AGC	0 : RFAGC OUT = "L", 1 : RFAGC OUT = "H" For details, refer to the Application Note.
IF. LOCK	Ignore because this does not function fully at present.
V. TRI	Returns the output of V trigger detection circuit in VCD. The internal memory status is renewed at every A. 1HEX : Detected
ST/NONST	Returns the output of V trigger detection circuit output in VCD standard (262.5 H) and NON standard. Returns in real time the FF output whose mode is determined in VCD. 1HEX : Standard For details, contact us after referring to the Application Note.
H. Lock	Detects the phase of FBP and Hsync, integrates the output, and detects in about 40H after HVCO LOCK. 1Hex : Locked
KILLER	Returns the color killer condition. However, the time constant is long, so that about 1V cycle (16 ms) is necessary for detection. Pay attention to the wait for change in the device status. Returns the real-time status for BUS Read. 1HEX : Killer ON
Color sys	Returns the color system status. Refer to the color system table in the register truth table. The read status is the same as for BUS Write.

Package Dimensions

unit : mm

3273